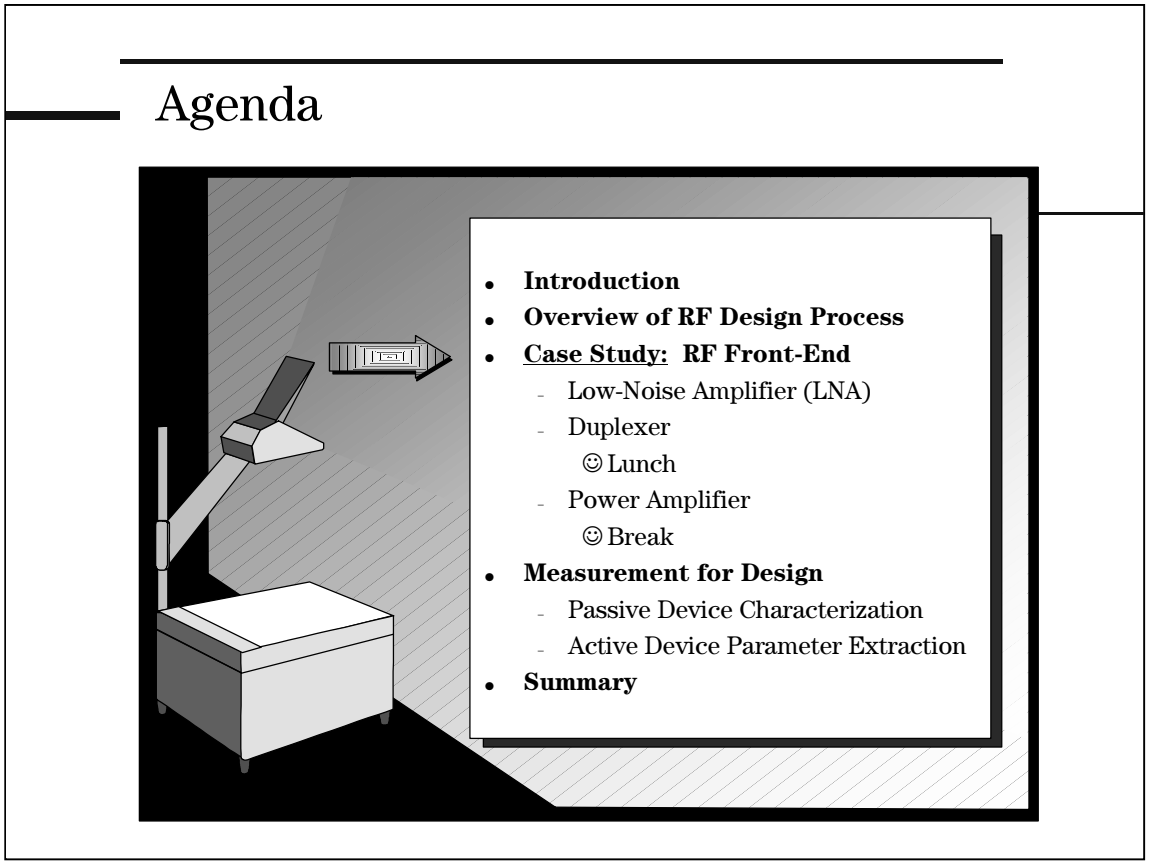
RF Design and Measurement Seminar

Slide #34



Now that we understand the RF design process, let's use it in the case study--the design and test of an RF front-end for a typical communications transceiver. The front-end consists of an LNA, power amplifier and duplexer on a single board.

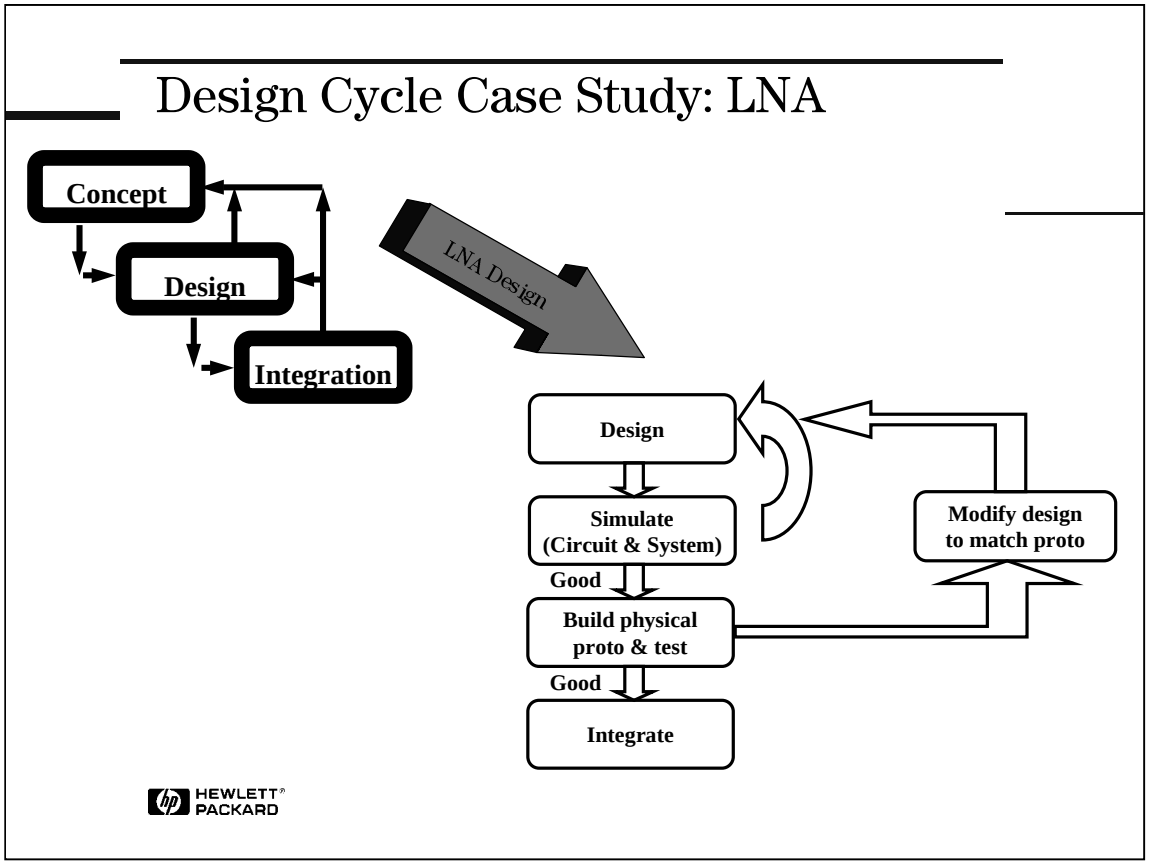
It is important to mention that the goal of this seminar is to present and implement the design methodology with the use of EDA software and test instrumentation, not to design the best LNA or even one with very realistic design constraints. Given our time constraints in creating and presenting this seminar, we have intentionally left out design constraints that you may have for your designs (e.g., physical constraints or power consumption).

You could design with additional constraints and use the same methodology to complete your work.

The software and test equipment we're using today have many capabilities that could take day/weeks to fully describe and demonstrate. Today, we're focusing on the basics. In time, and with experience, you'll learn more and become even more effective.

RF Design and Measurement Seminar

Slide #35



The previous section presented an abstract design methodology. Now, we'll look at a case study detailing the process used to design a PCS-band transceiver.

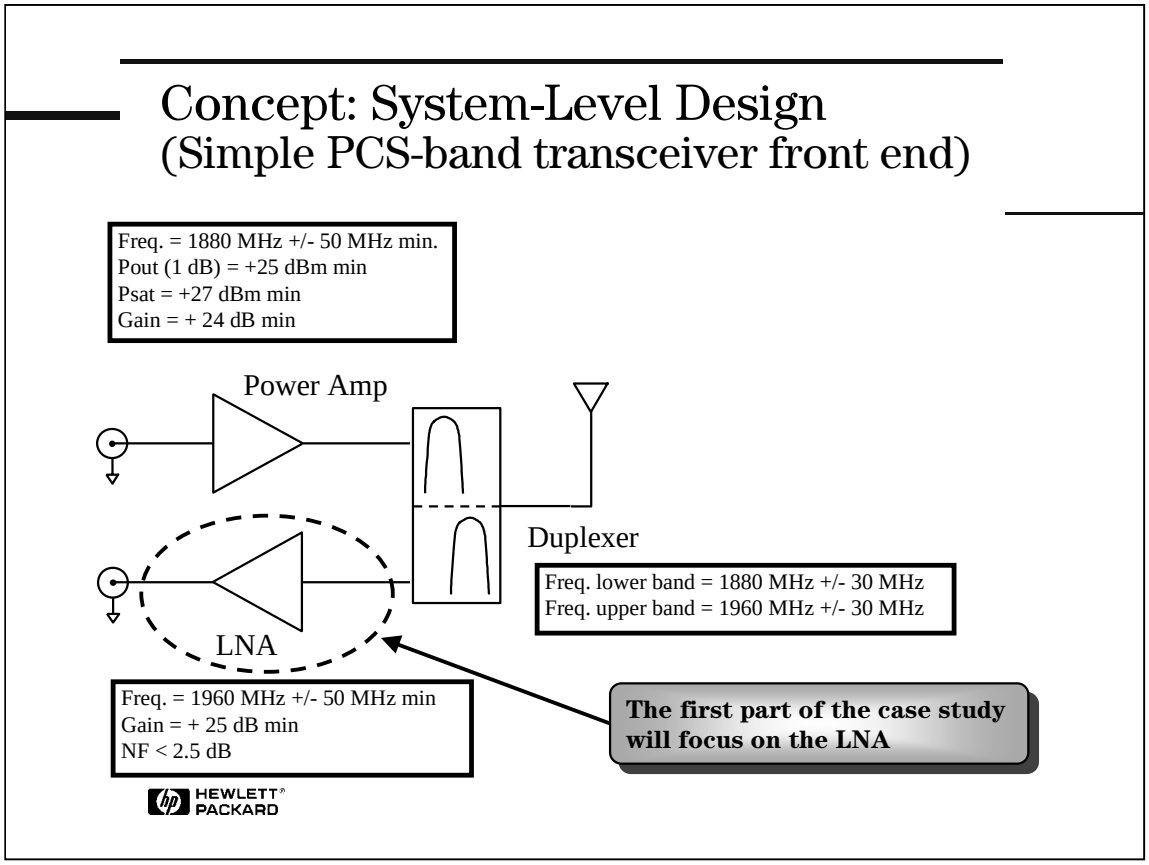
We assume that we have already gone through the concept, project definition, and investigation stage and have determined the specifications for the individual circuits.

We're going to begin with the LNA and demonstrate the design process using the modern predictive design methodology. The LNA is presented as a "common design" in which one encounters many problems normally associated with circuit design.

After covering the LNA, both the duplexer and power amplifier will be discussed. The power amplifier and duplexer will not be covered in as much detail as the LNA, but we will present the details related specifically to that individual design that were not covered in the LNA section.

RF Design and Measurement Seminar

Slide #36



The system-level block diagram shows the specifications for each of the individual parts of the transceiver. This diagram shows how each block is related to the others. The power amplifier must be able to produce a large amount of power, +27 dBm minimum in our case. The duplexer (two offset bandpass filters) is designed to transfer power from the power amplifier to the antenna and from the antenna to the LNA. Typically, the signal being received is low-power and as a result, it is important to add as little noise as possible to the signal as it is amplified.

The specifications of the LNA are: frequency range of 1960 MHz, +/- 50 MHz bandwidth, with at least 25 dB gain and a NF (noise figure) less than 2.5 dB. At the end of this section, we will see if these specifications were met with the first physical prototype.

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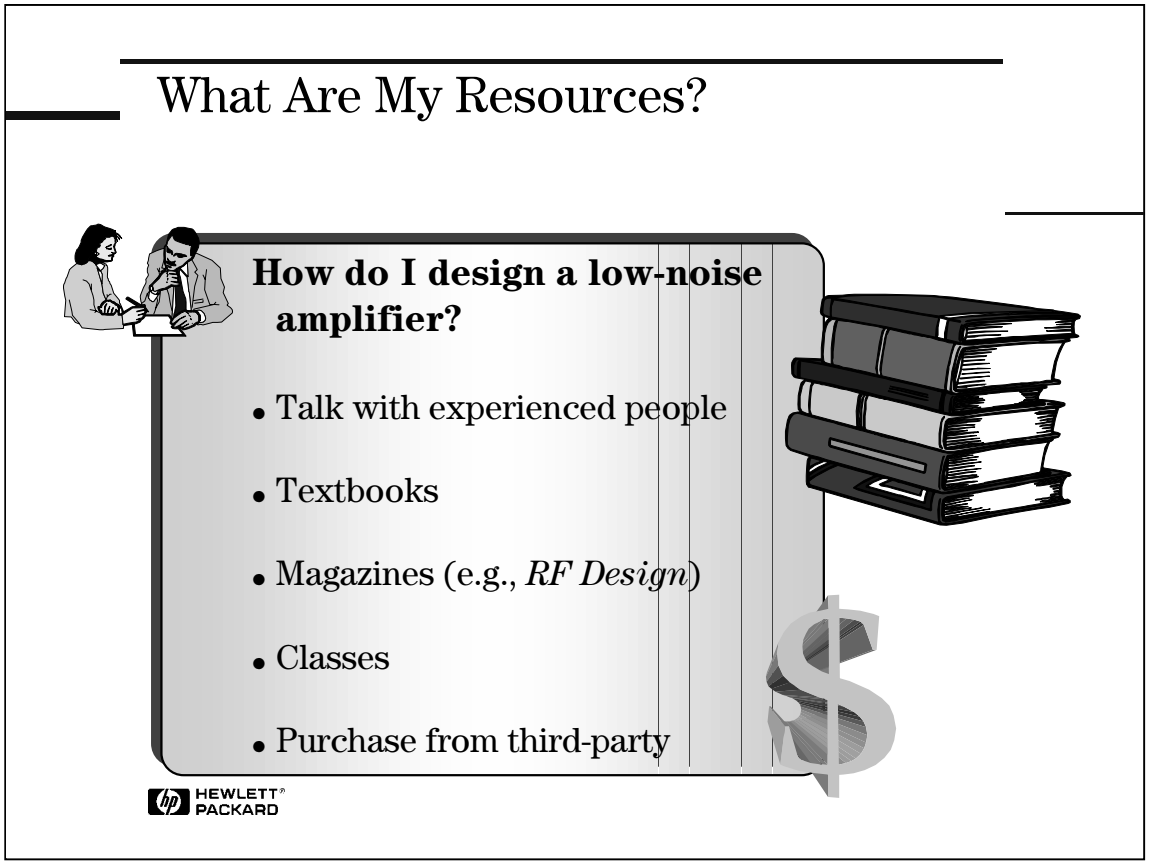
Slide #37



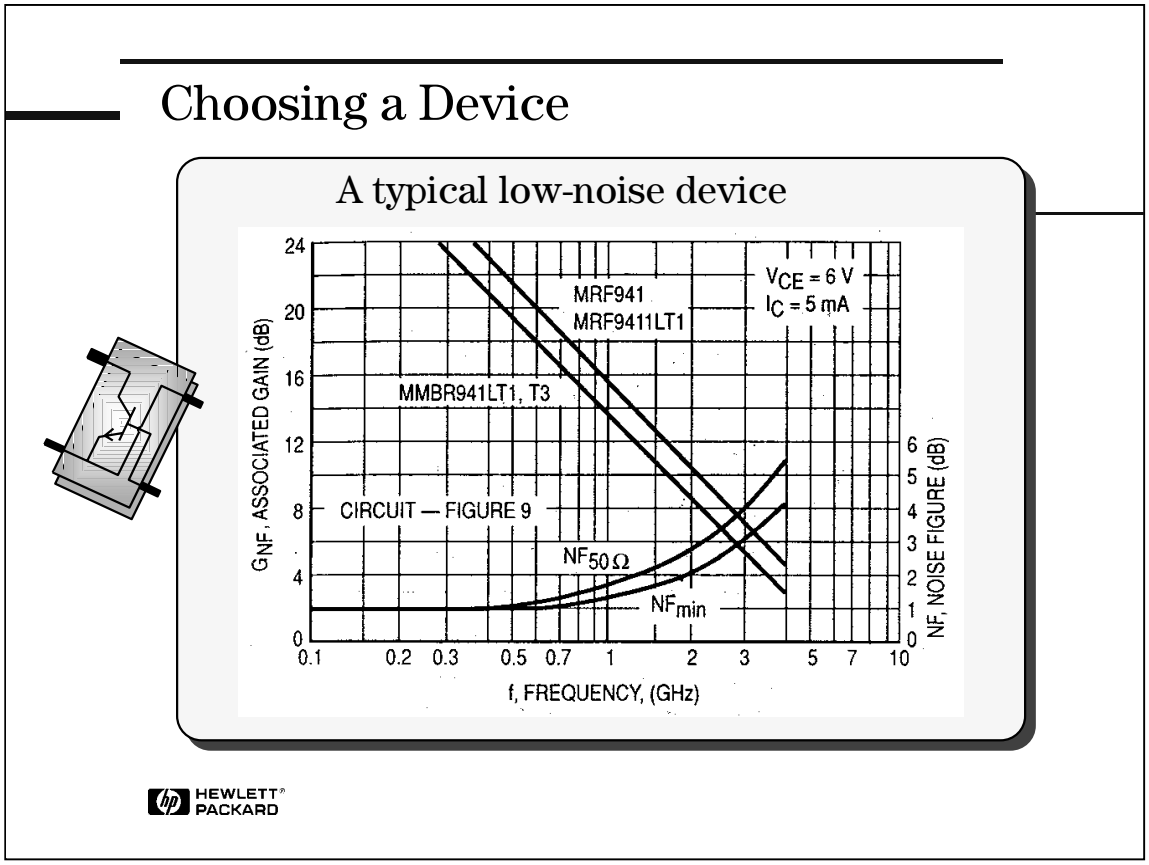
How does someone unfamiliar with RF design even begin designing an LNA? To begin with, it is important to know who and what your resources are. Often, the most useful information can come from someone who has done a similar design before. This person can be a wealth of information and can give you ideas and alert you to problems before you encounter them. This can save you, the designer, much time and effort later on. Most importantly, an earlier design is often the best place to begin a new design (redesign). Within HP, design reuse greatly reduces product development time.

Another excellent source of information can be technical books on the subject (i.e., college textbooks). The information is often more technical (as opposed to practical) and can be a very useful source of background information on the subject. Magazines and technical papers are a good way to get the latest information.

Finally, something that should be considered (but often isn't) is the decision to buy a product from someone else. People are often told that something is needed and they immediately start thinking about how to design it without even considering the fact that it could be bought. It is quite possible that the time and effort required to design something could be more expensive than purchasing a ready made unit from an outside vendor.

RF Design and Measurement Seminar

Slide #38



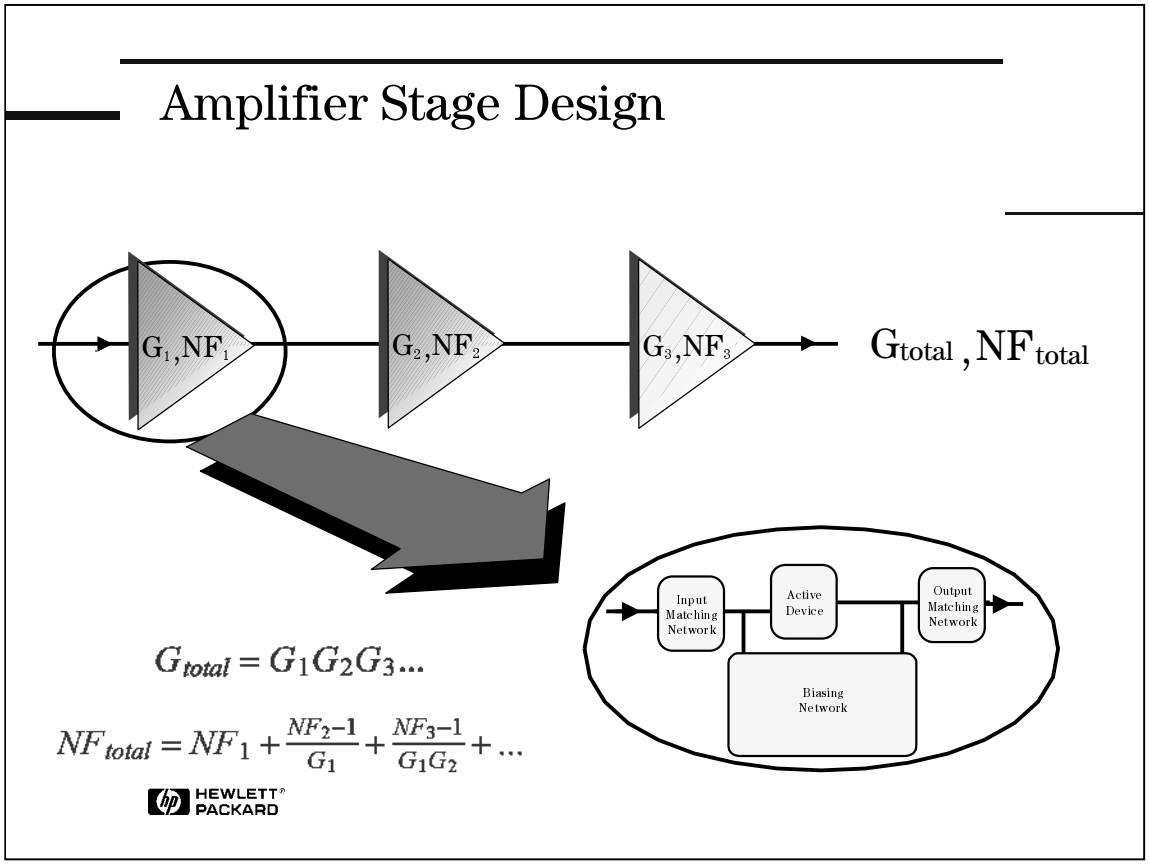
Once the overall requirements for the LNA have been decided, decisions on how to implement it must be made. Things such as device type, the number of stages required and the types of stages have to be determined. Next you need to decide on a topology (circuit design) and how the device(s) will be biased. Each of these steps will be discussed in great detail in the following slides. In this brainstorming portion of the process, major decisions on how to implement the LNA are made.

One of the very first things to do when designing a circuit is to decide on the active device to use. When doing this, you must take into account several factors, including availability. It may be necessary to use a transistor with poorer performance because it is stocked in your lab rather than wait for a better part. Long-term availability should also be considered (i.e., does the part come from a reputable vendor and does the vendor plan to continue production of the device). Price, of course, is always an issue as is package type. Most important are the device's specifications. This includes gain, noise figure, frequency range, power-handling capability, etc. The best place to find specifications is from a vendor's data sheet or catalog. Finally, your company probably has a preferred vendor/parts catalog. You'll want to make sure any part you use is approved.

Based on the requirements of our LNA, we chose to use two active devices: a low-noise BJT from Motorola (MRF9411) and a packaged HP MMIC (MSA-0386) as a general purpose gain block in a 50Ω system. We chose these devices because their specifications met our needs and were readily available in our lab.

RF Design and Measurement Seminar

Slide #39



Once the devices are chosen, the number and types of stages required to meet the specifications can be found. Using the Gain and Noise Figure equations for cascaded amplifiers, we see that the gain of the overall LNA is simply the product of the gain of each individual stage.

The equation for the total noise figure of a cascaded amplifier is a bit more complicated. The noise figure of the first stage adds directly to the overall noise figure, while the noise figures of subsequent stages are divided by the total gain of all stages before that stage. This means that the first stage performance of a cascaded amplifier is very critical to the overall noise figure.

The low-noise BJT (MRF9411) has a NF of 2.3 dB and the MODAMP has a NF of about 6.5 dB in our bandwidth of interest. The high NF of the MODAMP requires that the first two stages of the LNA be designed with the MRF9411. But since the gain of the MRF9411 is only 8-9 dB in our bandwidth of interest, a third stage will be needed. To get the desired gain, a third stage was added using the MODAMP. The lower noise figure of the device doesn't affect the overall noise figure much since the third stage has about 17 dB of gain before it.

Now that the devices for each stage have been determined, the topology of the various stages must be determined. Circuit topology refers to all portions of the circuit: the active device(s), the biasing network and the input/output matching networks.

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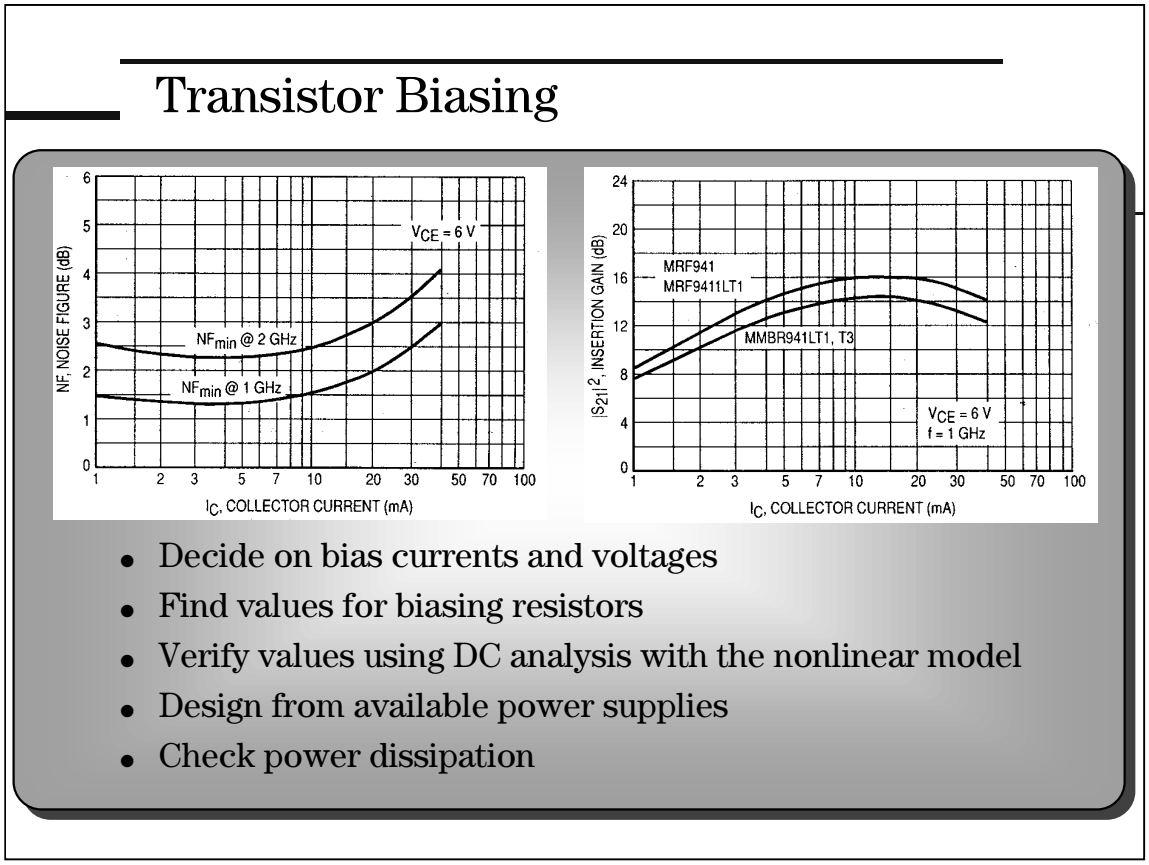
Slide #40



The biasing of the active device is a critical factor in the overall functionality of the design. Deciding the right biasing point for your device requires studying the specification sheets from the manufacturer. You can see from the graphs in the slide that there are several things to take into consideration. Gain and noise figure are both functions of collector current and (unfortunately) gain is not highest when noise figure is lowest. In our case, it is critical for the first stage to have low noise and since we should have plenty of gain with three stages, we decided to not maximize the gain, but rather to minimize the noise. Therefore, we chose a bias point of Ic = 5 mA.

Next, we find values for the elements of the bias network. There are a couple of things that must be kept in mind when you are designing the bias network. First, what voltages are available on the board? Make sure your biasing works with the voltages available. Finally, check for power dissipation in biasing resistors to make sure that power specifications are not exceeded. Some resistors may dissipate too much power for SMT, and a through-hole resistor with a high power rating may be required. Check your design with DC analysis. Back annotation to the schematic will show node voltages and branch currents.

HP offers a free utility called AppCAD, which can help with designing bias networks. Information on AppCAD can be found at http://www.hp.woodshot.com.

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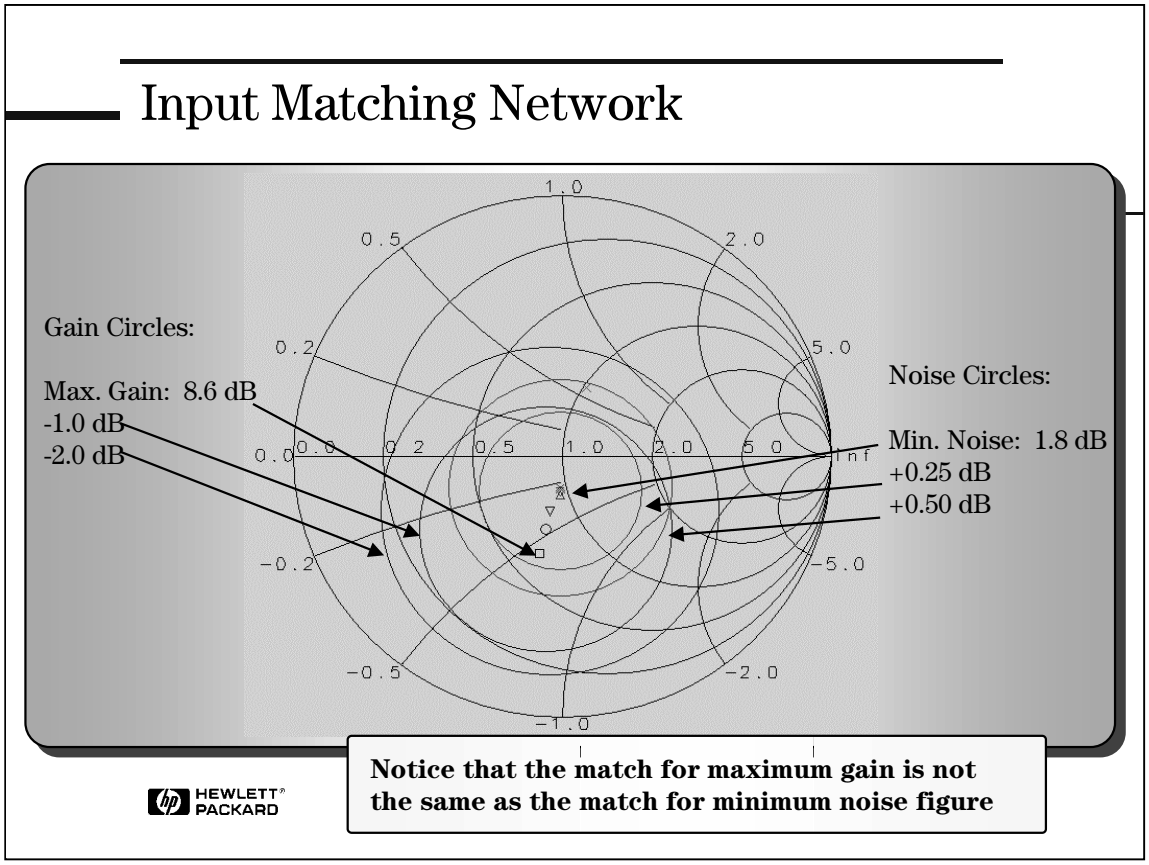
Slide #41



After the transistor is biased, the next step is to design the input matching network. EDA software such as HP Advanced Design System will create noise and gain circles showing the impedance necessary to deliver the displayed gain or noise figure.

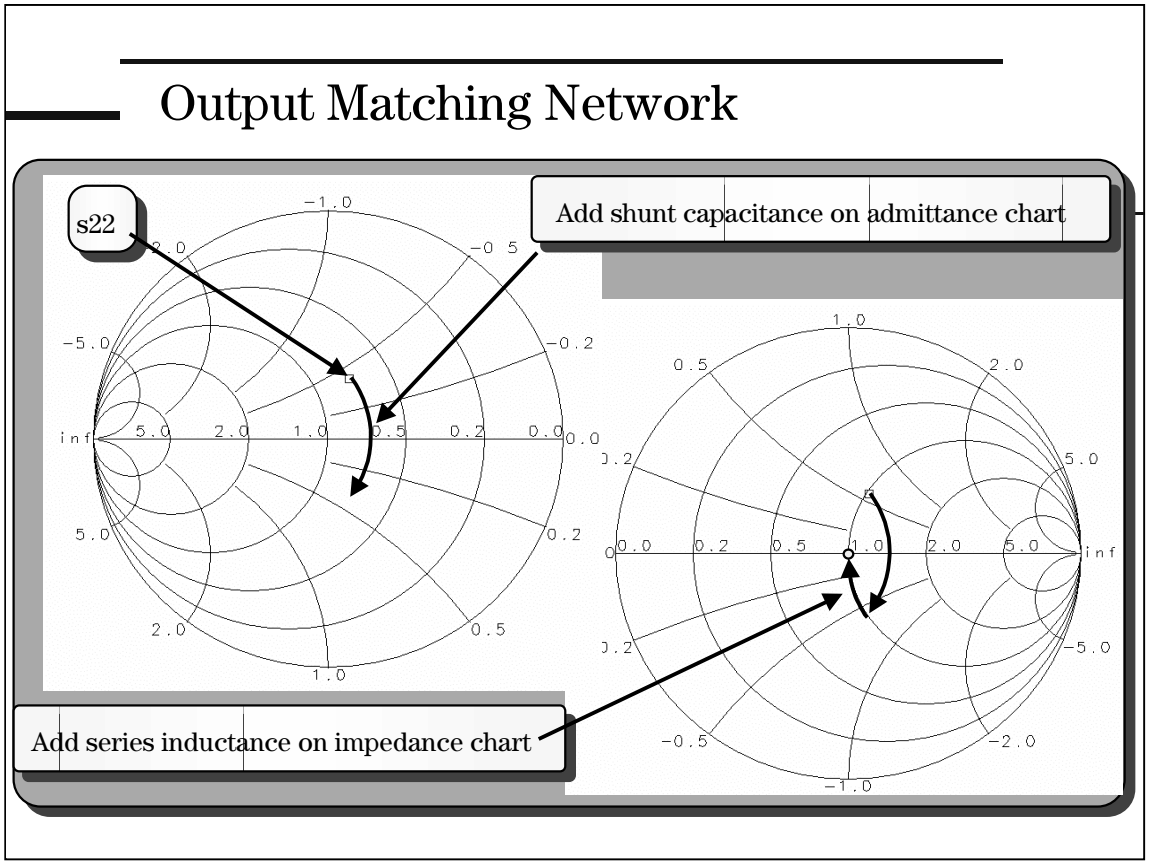
We can see that, generally, it is not possible to simultaneously match the device for both minimum noise figure and maximum gain. As a result, there will have to be a trade-off between noise figure and gain.

For the output match we want to deliver the maximum power to the next stage. This is accomplished by presenting the output of the transistor with an impedance that is the complex conjugate of S_{22}.

Once we have decided upon impedances to present to the input and output of the transistor, the problem becomes how to create a matching network that presents this impedance to the input/output of the device.

RF Design and Measurement Seminar

Slide #42



Once an impedance has been found on the Smith chart, how is a matching network that will provide that impedance designed? There are several ways to implement this matching network depending on your circuit. The first method uses lumped reactive elements to provide the match. This method is typically used for lower frequency designs or when you have space constraints.

The goal of the matching network is to transform the impedance of the device to a desired impedance. We want to transform the S_{22} of the device to 50Ω. Graphically, take S22 and transform it, using either transmission lines or reactive elements, to the center of the Smith chart (a perfect 50Ω match).

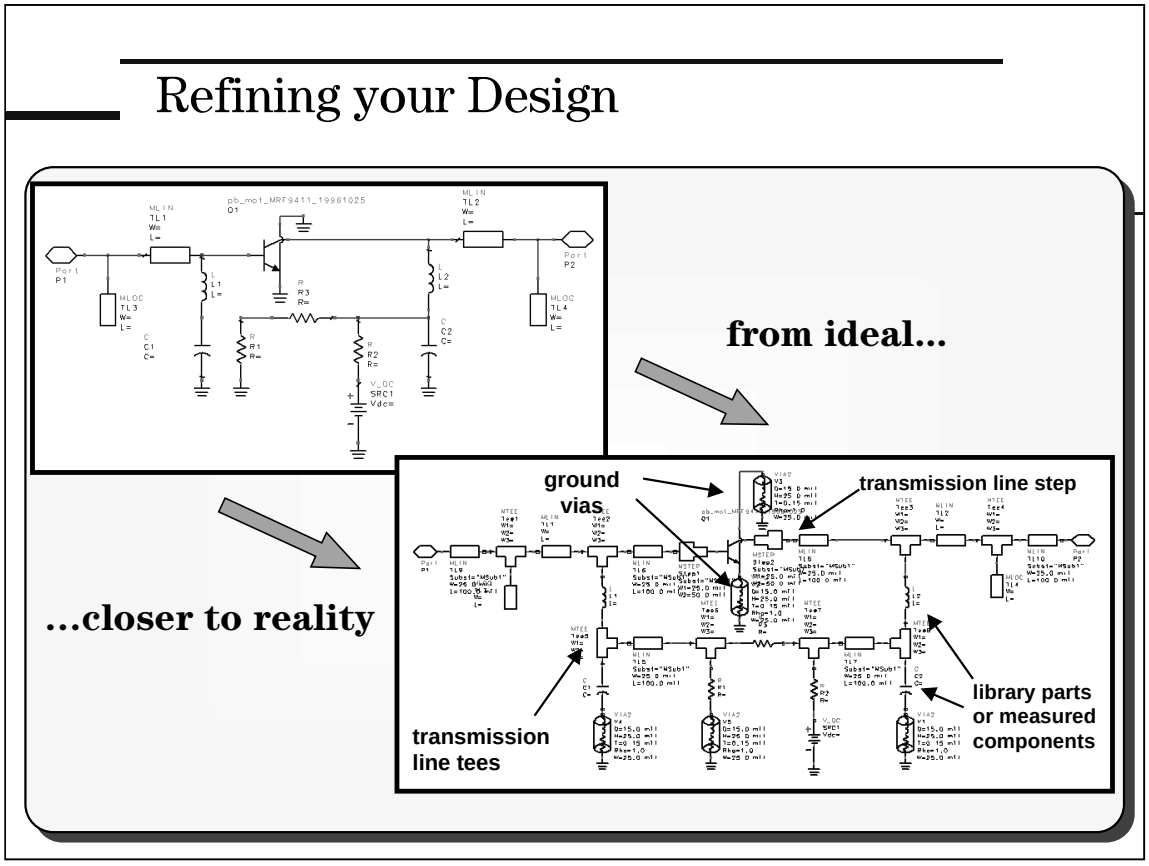
We used the admittance markings on the Smith chart and moved the output impedance onto the unity circle by adding shunt capacitance. Once the impedance is on the unity circle, use the impedance markings to add series inductance until the impedance is at the center of the circle.

The other method that was used in this LNA design is distributed single-stub tuning. This matching technique uses a single open-circuited or short-circuited length of transmission line (a "stub") between a length of transmission line leading from the device to the transmission line you are matching.

Be aware that S22 shown on the slide is for one frequency only. Each frequency will have a different S22, and as a result, S22 will actually be a trajectory over the bandwidth of interest. This means that it is impossible to perfectly match the output over the complete bandwidth.

RF Design and Measurement Seminar

Slide #43



Here's what the design looks like after we've created the bias and input and output matching networks. Beginning your design with ideals allows you to determine from the start if the specifications are unrealizable. But it is important to acknowledge that although we have created what appears to be a working design, it is only an ideal design.

Next, you'll want to begin refining your circuit design to include non-ideal parts as well as their physical interconnection.

The microstrip transmission lines as well as the lumped components are physical elements that need to be interconnected with microstrip. And any discontinuities in these connections need to be modeled with tees and steps. Vias through the substrate to ground needed to be added. Other interconnections and output microstrip lines may also interact with your design. Models for component footprints should be added since their size adds parasitic capacitance.

Finally, you may find that some components need to be measured directly. If the part you want to use does not have a model in the parts library or if it was created under different or unknown operating conditions, you will need to measure those parts. Sensitivity Histograms (covered later) may show that your design's performance is very sensitive to a certain part. These critical components may also need to be measured directly.

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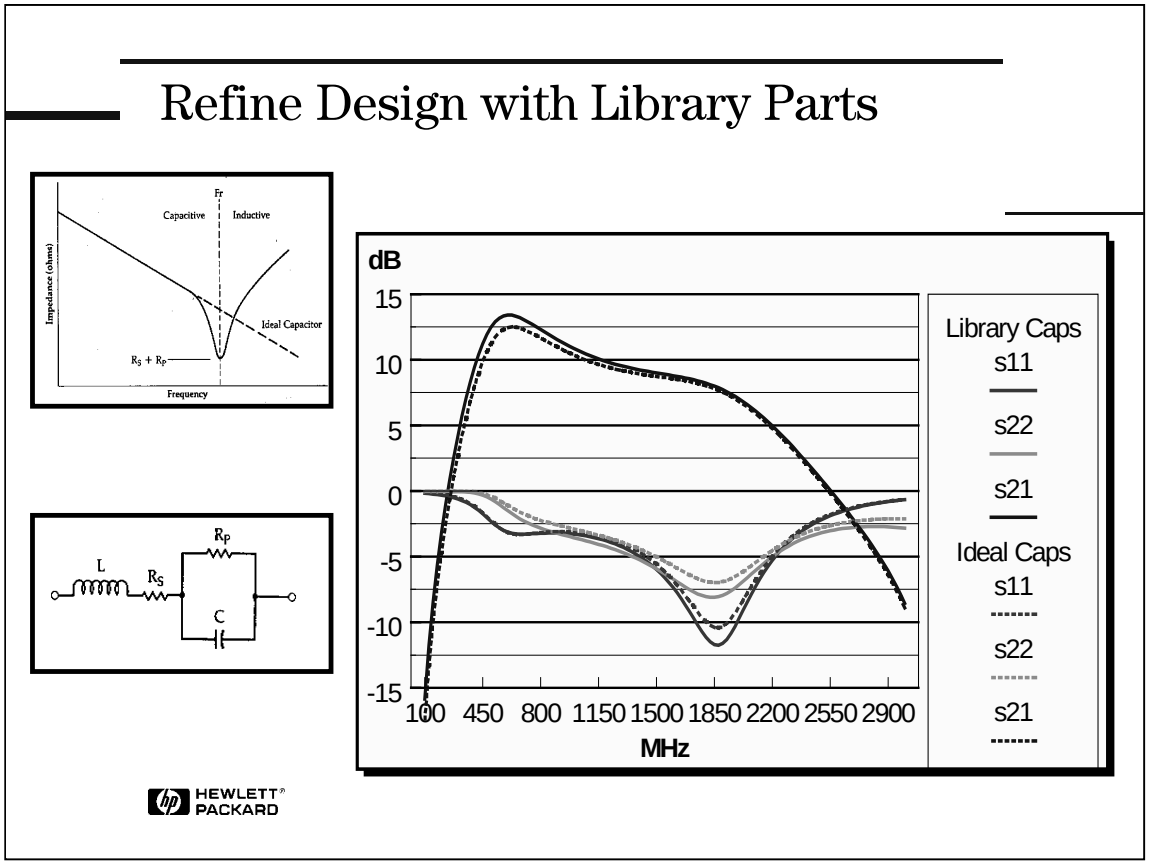
Slide #44

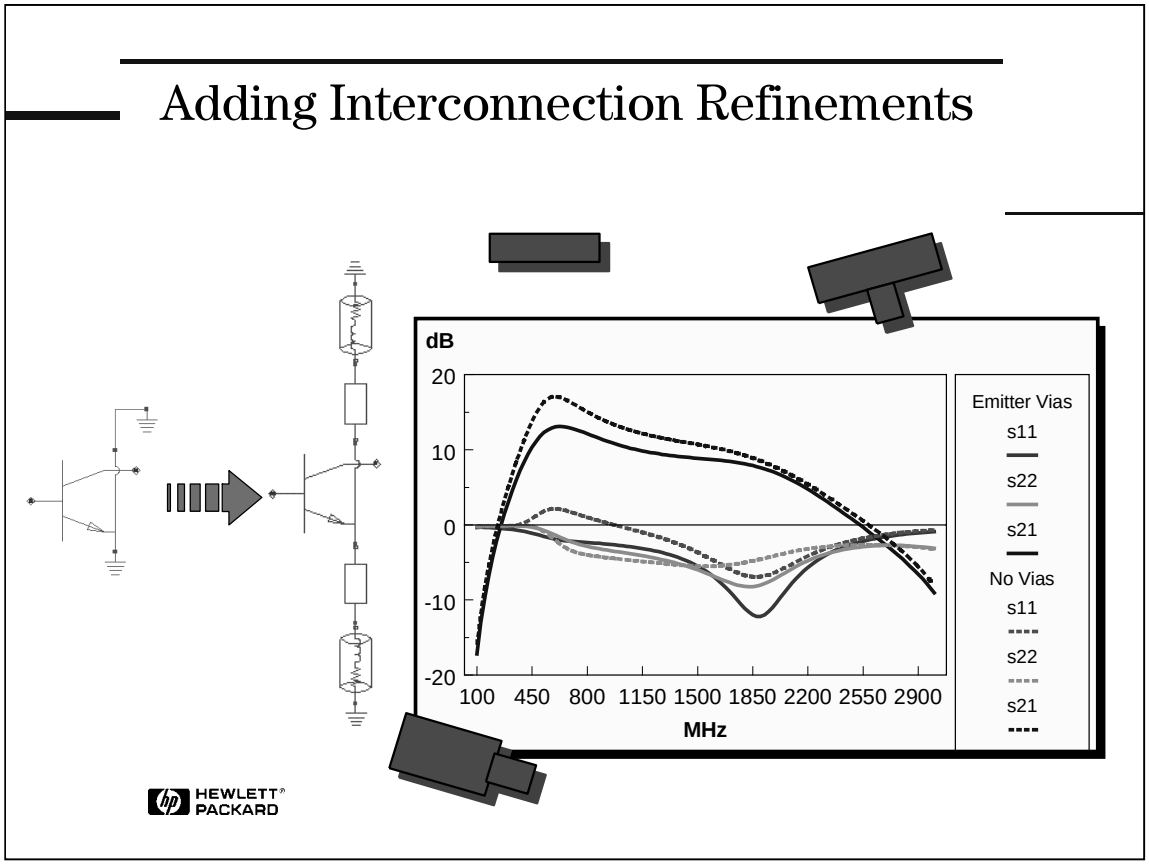


At higher frequencies, all ideal components become RLC circuits. Even a wire will start to have some inductance and capacitance and will need to be replaced with a transmission line. These parasitic inductances, capacitances, and resistances can have a significant effect on the performance of your design. Notice how the actual capacitor acts like a capacitor at lower frequencies, reaches resonance, and then at frequencies above the resonance it acts like an inductor.

The first elements in the design we refined were the capacitors. All the capacitors in the circuit were converted from ideal capacitors to library parts. These library parts are either data files containing linear data provided by the component manufacturer or closely matched equivalent sub-circuit models. You can see from the slide that there is about 2 dB of difference between matches and little difference in the gain between ideal and library capacitors.

RF Design and Measurement Seminar

Slide #45



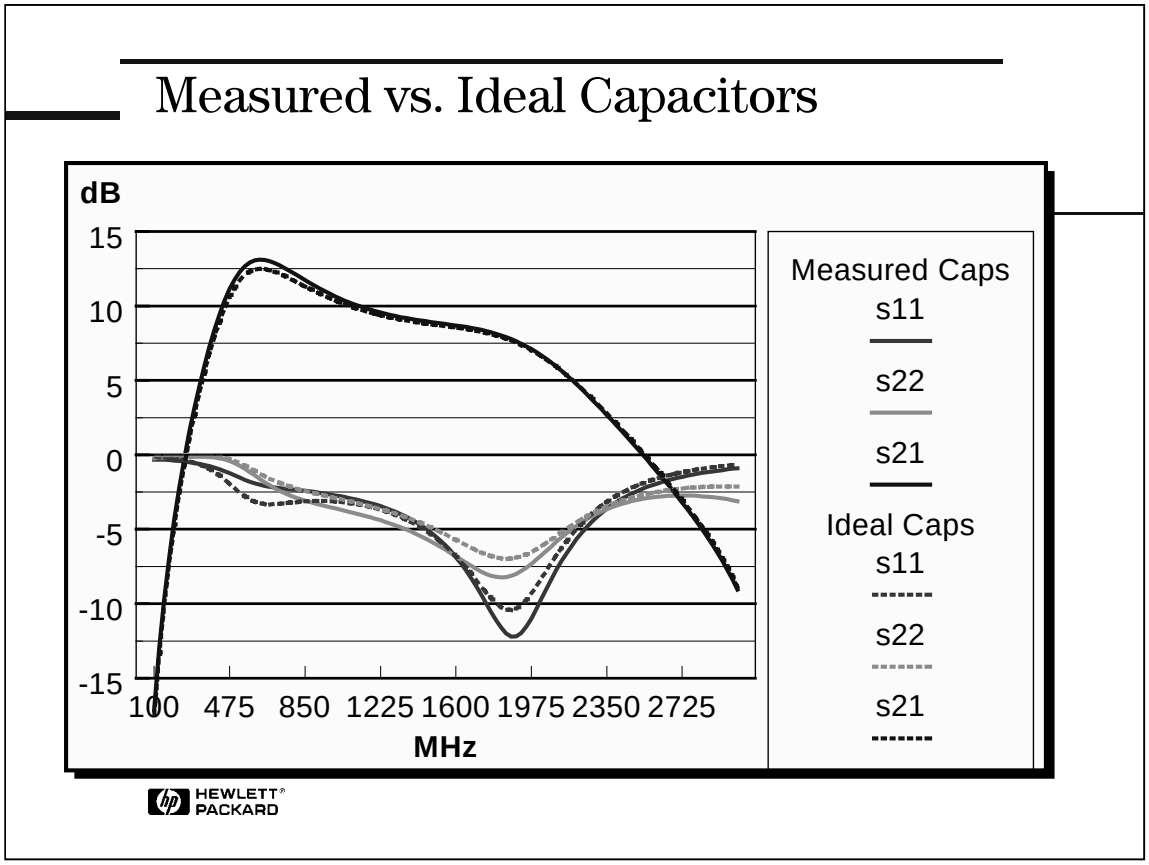
After adding library components to the design, we added tees and steps that model microstrip discontinuities. These discontinuities become increasingly more significant as the operating frequency of the design increases.

Vias can also have a large affect on circuit behavior. The board has some thickness, and ground is usually on the opposite side of the board from the components: via models account for the thickness of the board and parasitic resistance and inductance. One sees that the added inductance associated with the vias can greatly affect circuit performance. Not including vias in your simulation could make you think that your gain will be better than it actually would be. And in many cases, the parasitic inductance of a via on a transistor's emitter ground is used to improve stability.

It is important to keep the objective in mind: to include in the design physical characteristics that will exist on the physical board. Implied in this process is that uncontrollable parasitic or "undesired" effects should not be massaged or deleted. The undesired parasitic effects will always be there and you must design around these.

RF Design and Measurement Seminar

Slide #46



What happens if the library part doesn't match your component, was measured under different conditions, or was measured under unknown conditions?

An extremely important part to the design cycle is the measurement of components. Earlier, we were shown the effects non-ideal parts can have on a design. When a component you are using in the circuit isn't included in the library, or if it was measured under different conditions, it is necessary to measure the component.

With EDA software such as HP Advanced Design System, you can connect your PC or workstation to a network analyzer and read the measured data directly.

In our LNA design, we were unsure who the vendor of our capacitors was, so we measured them.

The circuit behavior changes when the measured capacitors are included instead of ideal capacitors. The match varies about 2 dB, but we don't see much change in the gain.

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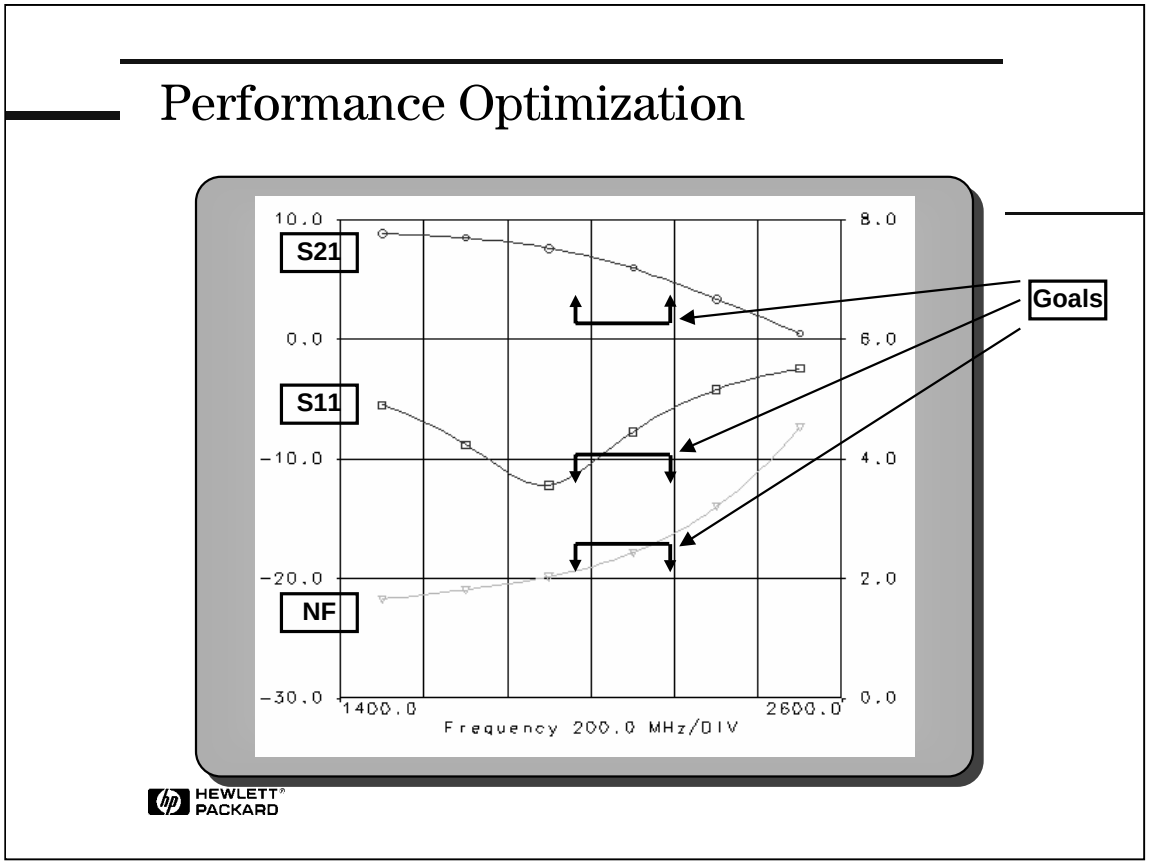
Slide #47



Now that we have modified our design to be more realistic, these modifications have changed the performance of the ideal LNA.

An easy and powerful way to adjust your design to improve its performance and meet specification is through performance optimization.

Optimization works as follows:

1) specify the goal or goals (e.g., the first stage of our LNA has the following specifications S11<-10 dB, S21 > 6.5 dB and NF <2.5 dB)

2) specify the components and the parameters that can be modified (e.g., length of microstrip or values of capacitors and inductors).

3) the EDA software searches out the parameters that meet your goals

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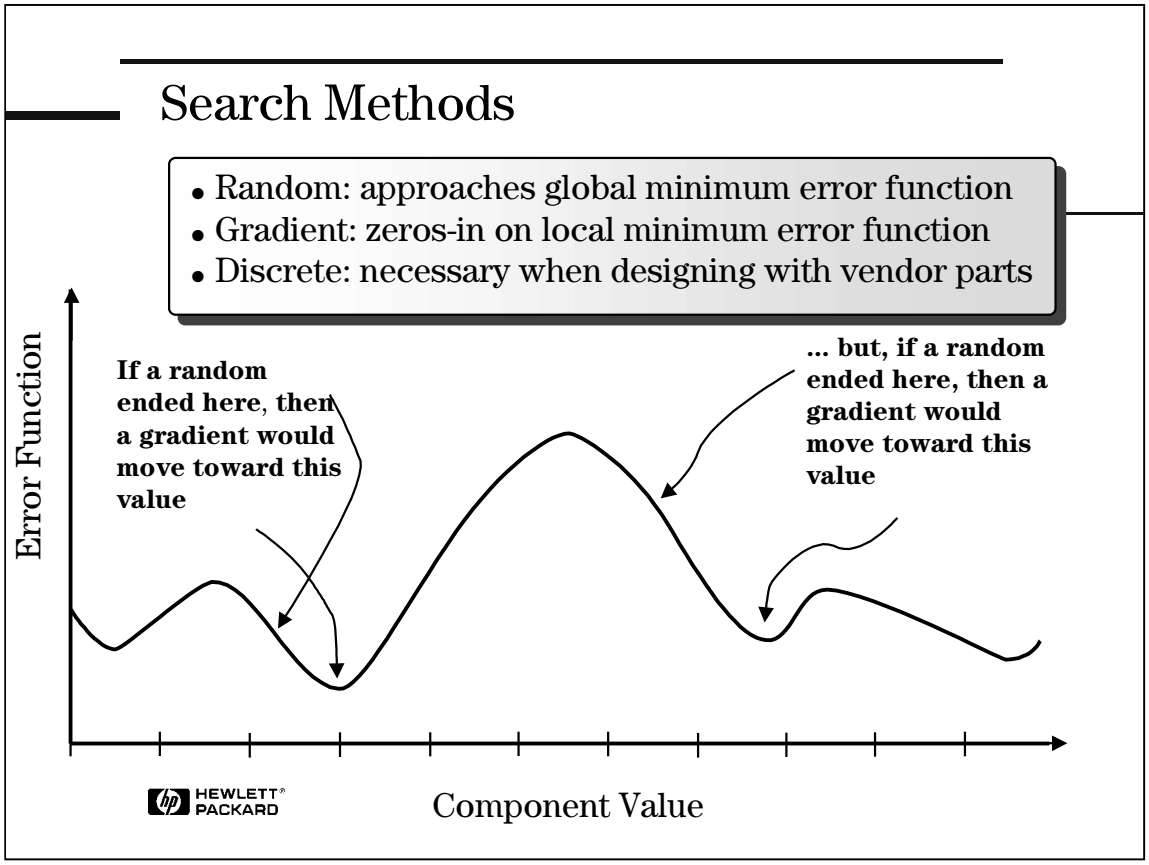
Slide #48



When optimizing, you have a number of different search methods to choose from. The two most commonly used are random and gradient searches. In a random search, design variables are initially randomly perturbed in an effort to minimize an error function (difference between simulated results and the goals). This method of searching tends to overcome problems with local error function minima. A gradient search uses directional derivatives and small perturbations to search for local minima. This has the advantage of zeroing in on minimums close to where the search started from. Typically, when beginning an optimization, a combination of random and gradient searches is used.

There are several other types of search methods, sometimes also referred to as optimizers. The most powerful is the discrete optimizer, which allows only discrete values. This type of optimization is necessary if you are designing with lumped components such as inductors, capacitors, and resistors because these parts are usually only available in discrete values. With the discrete optimizer, only realizable values (available from the vendor) are used .

Also, EDA software assumes that the TEM mode is excited in the microstrip transmission lines. If dimensions are used that may excite a different mode, the results of the simulation may be invalid. EDA software will warn you when you are using values that are not valid for the element models you are using.

A good rule of thumb: keep the width of the stub to less than one-half its length.

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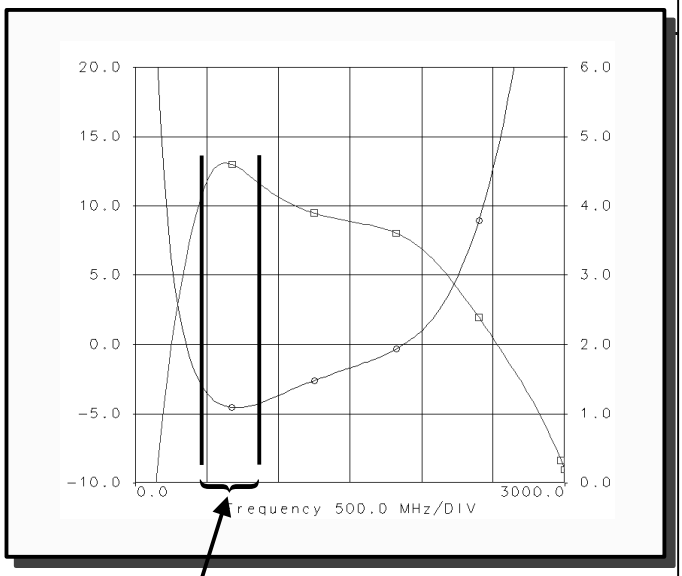
Slide #49

Problems with the Breadboard

Things to look for when troubleshooting:

- Stability at all frequencies
- Biasing problems
- System interactions



region of possible oscillation

HEWLETT PACKARD

At this point in the design process, you can be quite certain that any problems showing up in the software will show up in the physical prototype as well. This is the real power of the modern predictive design methodology. When you see a problem, it is easy to go in and quickly redesign without building a prototype to realize that there is a problem.

Discovering problems requires some knowledge of what to look for. For LNA designs, we want to make sure we are designing an amplifier and not an oscillator! Stability at all frequencies (not just the frequency range of interest is of primary concern in addition to the design specifications. Power dissipation in the biasing network may be another problem. Interactions with the higher system-level design should be explored.

In our LNA design, it became apparent that there was a problem in the 400-500 MHz range. There is a gain peak in this area, in addition, the stability factor of the circuit (not shown) went below unity in this area, indicating conditional stability. This 400-500 MHz region shows a suspected oscillation.

Let's fix this problem before we build the board.

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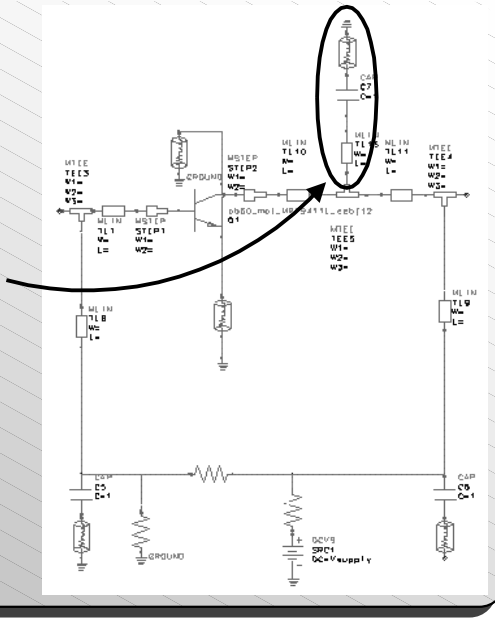
Slide #50

Removing the Oscillation

Hypothesis: collector impedance is too high at lower frequencies

- Remove oscillation by lowering collector impedance at problem frequencies (while maintaining correct impedance in the desired band)
- Shorted stub on the collector



HEWLETT PACKARD

This is actually a very typical problem in amplifier design. The standard approach to reduce the possibility of oscillation is to reduce the impedance in the frequency range where you may have the problem. We decided to try reducing the impedance at the collector of the transistor by using open and shorted stubs, although we could have tried reducing the impedance at the input as well.

Being careful to allow only the lengths of the transmission lines around the stub and the stub itself to vary, we optimized for stability. The gain at the lower frequencies was significantly reduced and the stability was greater than one for all frequencies, indicating that the circuit was unconditionally stable.

It's important to control which components and parameters you allow to vary. If you allow all components and parameters to vary, other parts of your design could be adversely affected, or the optimizer may not find a useful solution at all.

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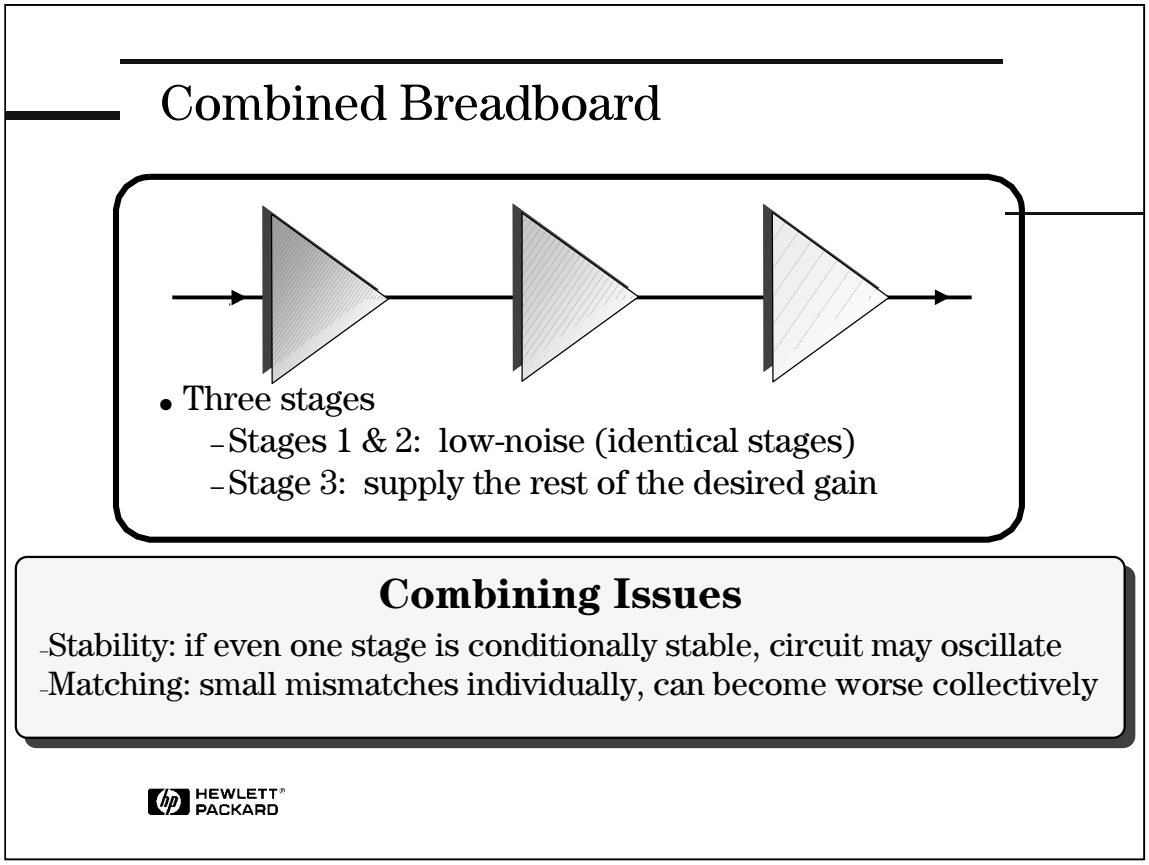
Slide #51



Now that the first stage has been designed and meets our design goals, the remaining stages need to be added. The second stage, which needs to be low noise as well, was simply a duplicate of the first stage. The third stage used to provide the remaining gain was a simple MODAMP design. Since it is a packaged device matched to 50Ω, the design mainly consisted of a small biasing network.

You should also be aware of stability when cascading amplifier circuits. Unless all stages are unconditionally stable, oscillations can occur when the stages are put together even though they do not oscillate by themselves. Mismatching can lead to problems when cascading amplifiers. Small mismatches on an individual stage can become worse when combined with another circuit with some mismatch.

Up until now, we've focused primarily on logical design with our schematic. Now let's focus on the physical design with the layout. EDA software such as the HP Advanced Design System has an integrated layout that makes it easy to generate the physical design artwork for building the prototype.

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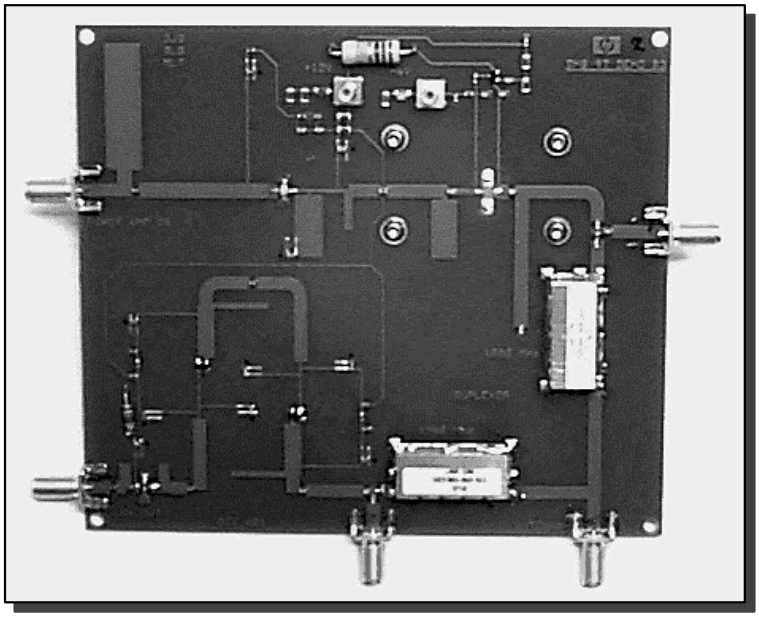
Slide #52

Build the Prototype

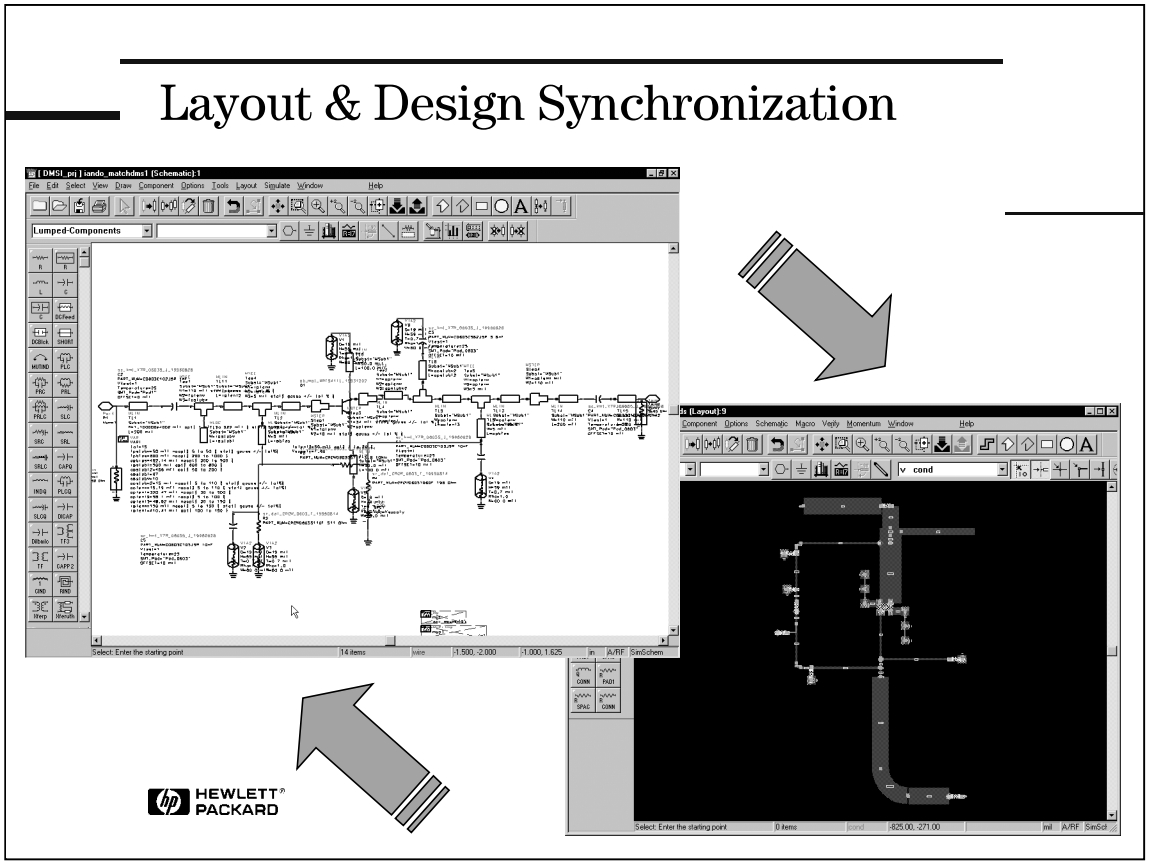


HEWLETT PACKARD

Layout of your logical design is the first step in the manufacturing process. In the traditional design process, the layout is typically performed by EDA software, but is usually not integrated with the logical design and simulation software. Now, with EDA software such as HP Advanced Design System, schematic and layout are available in a single environment. Even if you use some other software for production, EDA software can either export the artwork into your production process or, in special cases, the designs can transfer directly to our back-end manufacturing process.

RF Design and Measurement Seminar

Slide #53



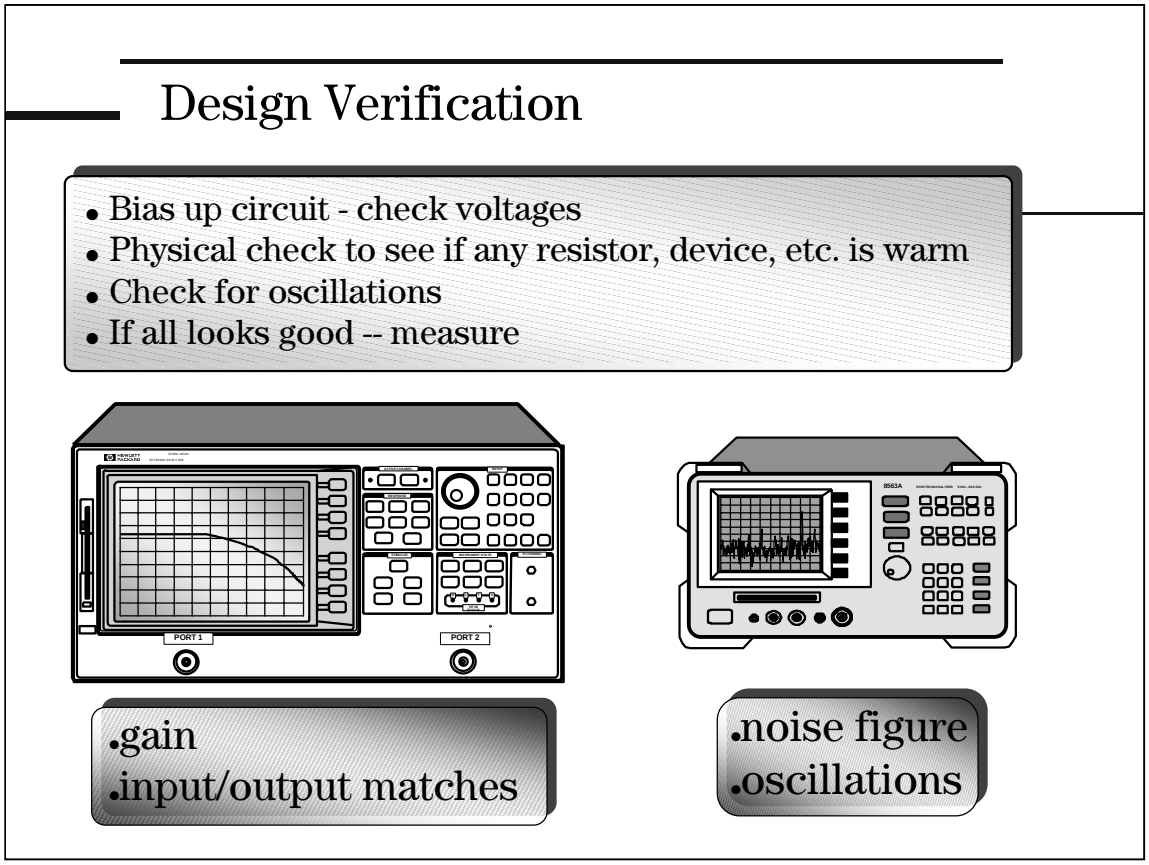
EDA software makes layout of your design easy with design synchronization. Design Synchronization allows you to place components from the schematic to the layout, make changes in either, and have the changes updated in the other representation.

For example, to keep the area somewhat confined, we used bends in the microstrip. These were added in the layout. The changes are automatically made to the schematic and can be resimulated to make sure that the performance has not been adversely affected.

It's also easy to visually check your design for realizable microstrip lengths and widths. You can also set up design rules such as how close you'd like to allow components to get to each other and have them checked automatically.

RF Design and Measurement Seminar

Slide #54



Once the prototype has been built, it is time to measure its performance. Before you measure the S-parameters and the noise figure, though, you'll need to check for proper biasing and power dissipation. The network analyzer measures the most important parameters of the circuit: gain, match, and group delay. A spectrum analyzer measures nonlinear parameters such as noise figure and TOI, and can detect distortion products.

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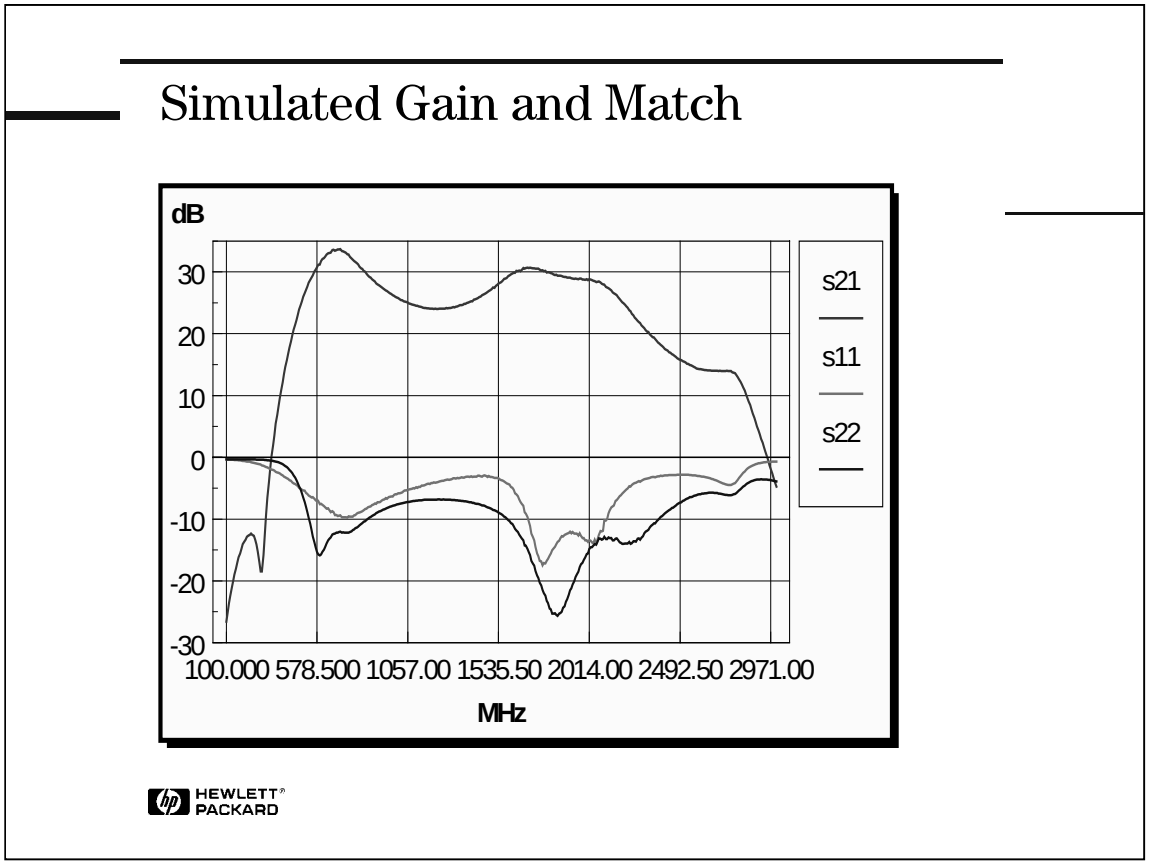
Slide #55



Here are the simulation results of the three stage LNA. S11, S22 and S21 are displayed. We're interested in the performance from 1910 MHz to 2010 MHz. Over this frequency range, it looks like we'll meet the design specifications for the LNA.

Simulated results over the specified frequency range:

S11 < -10 dB

S22 < -10 dB

S21 > +25 dB

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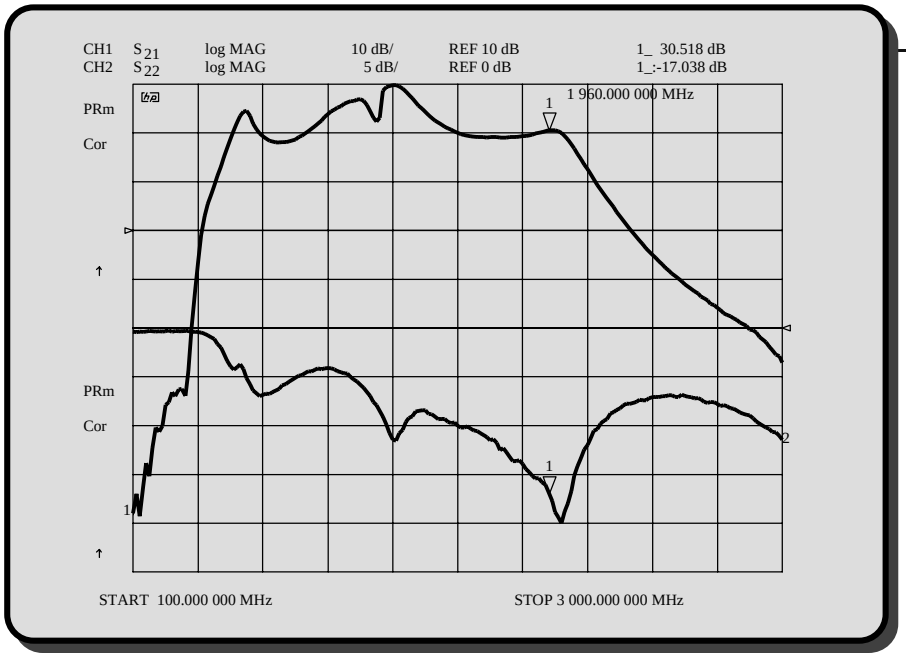
Slide #56

Measured Gain and Output Match



When we measure S11 and S22, we find that the S11< -11 dB and S22 < -16 dB. Similar to the simulation results and better than spec. And when we look at gain, S21 > +30 dB. Again, better than specification and similar to the simulation results.

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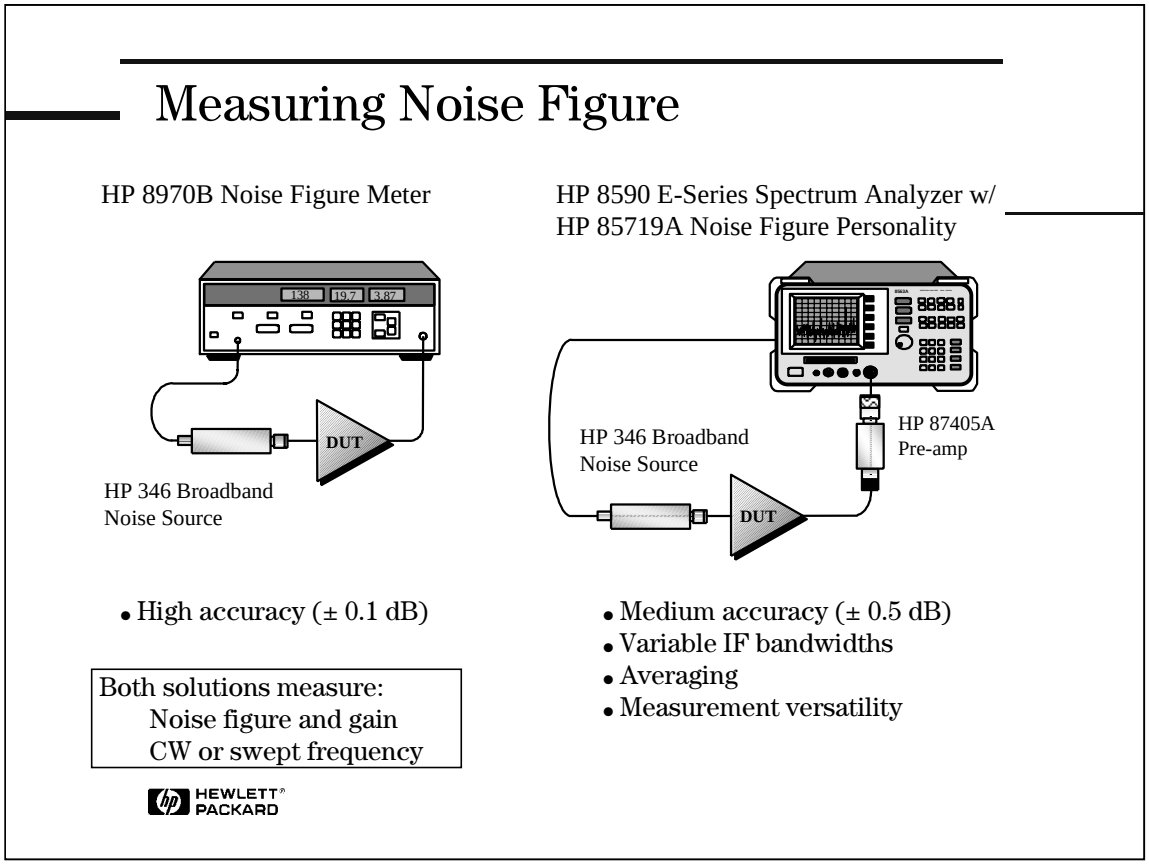
Slide #57



A broadband excess-noise source and a narrowband tuned receiver can be used with the Y-factor technique to characterize the noise figure and gain of an amplifier versus frequency. There are two common measurement receivers used as the tuned receiver: dedicated noise-figure meters and spectrum analyzers.

Noise-figure meters such as the HP 8970 series generally provide the most accurate results compared to other alternatives (typical measurement uncertainty is ±0.1 dB). They provide both CW and stepped-frequency measurements, with excellent measurement speed. The RF noise-figure meter (HP 8970B) can be combined with a microwave test set (HP 8971C) for coverage up to 26.5 GHz. An integrated microwave system is available (HP 8970S/V), which includes an RF source used as a local oscillator (LO).

While spectrum analyzers can be used manually to measure noise figure, an option is available for the HP 8590E series spectrum analyzers to greatly simplify the measurement procedure. This option is the HP 85719A noise figure measurement personality, and it measures both noise figure and gain versus frequency. Accuracy is respectable, but not quite as good as a dedicated noise figure meter (typical measurement uncertainty is ±0.5 dB). A few accessories are needed with the personality, such as the excess-noise source (HP 346B), a low-noise preamplifier to improve the overall system sensitivity (HP 87405A, 10 MHz to 3 GHz), and Option 119 for the spectrum analyzer.

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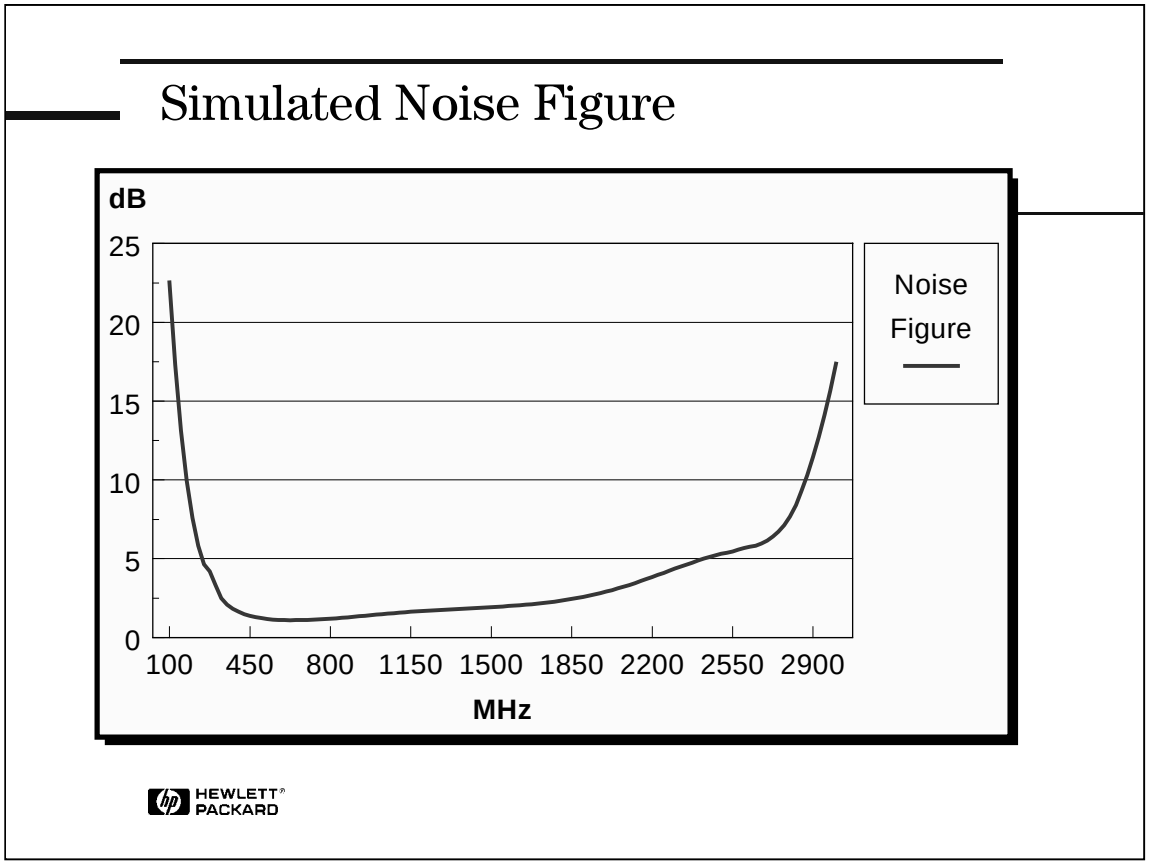
Slide #58



Here are the simulation results of the noise figure of the three-stage LNA.

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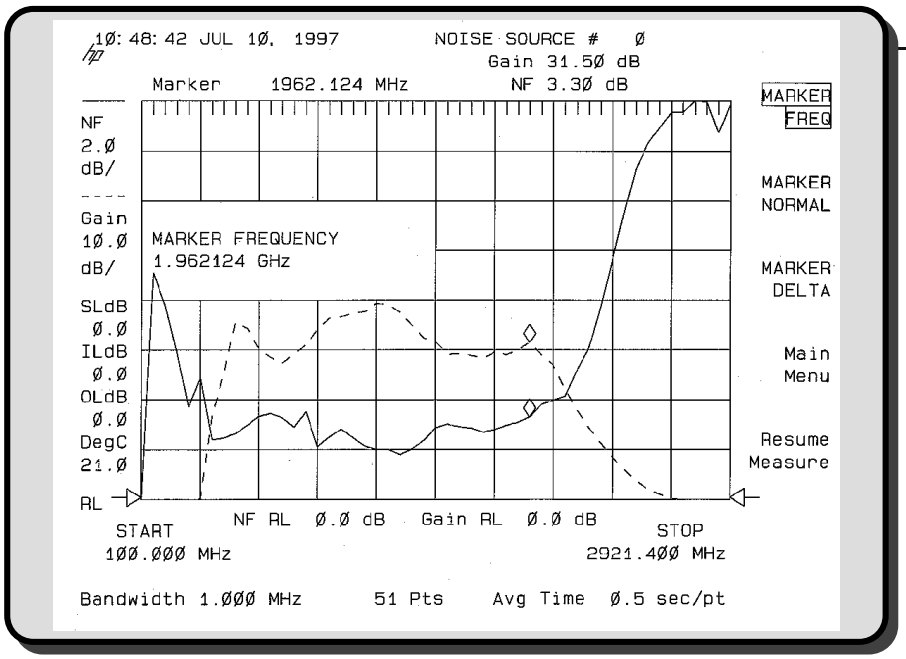
Slide #59

Measured Noise Figure



The measured noise figure is 3.3 dB.

This is an odd result and doesn't meet specification. Let's look back at the NF equation:

$$NF = NF1 + (NF2-1)/G1 + (NF3-1)/(G1G2)$$

Since we know that the NF is heavily dependent upon the gain of the first stage and the noise figure of the transistor, we may have had a device that didn't meet specification or that had a parasitic we didn't anticipate.

Examining the design, we found that the dimensions of the microstrip lines as built were not the same as the ones we specified in the design. During our manufacturing process we didn't use the automatic layout capability within the HP Advanced Design System and relied upon a manual layout re-entry process to enter the design. As such, some errors were made and the LNA was not built as designed. When we went back to modify the design to reflect how it was built, we got the same noise figure results as we measured.

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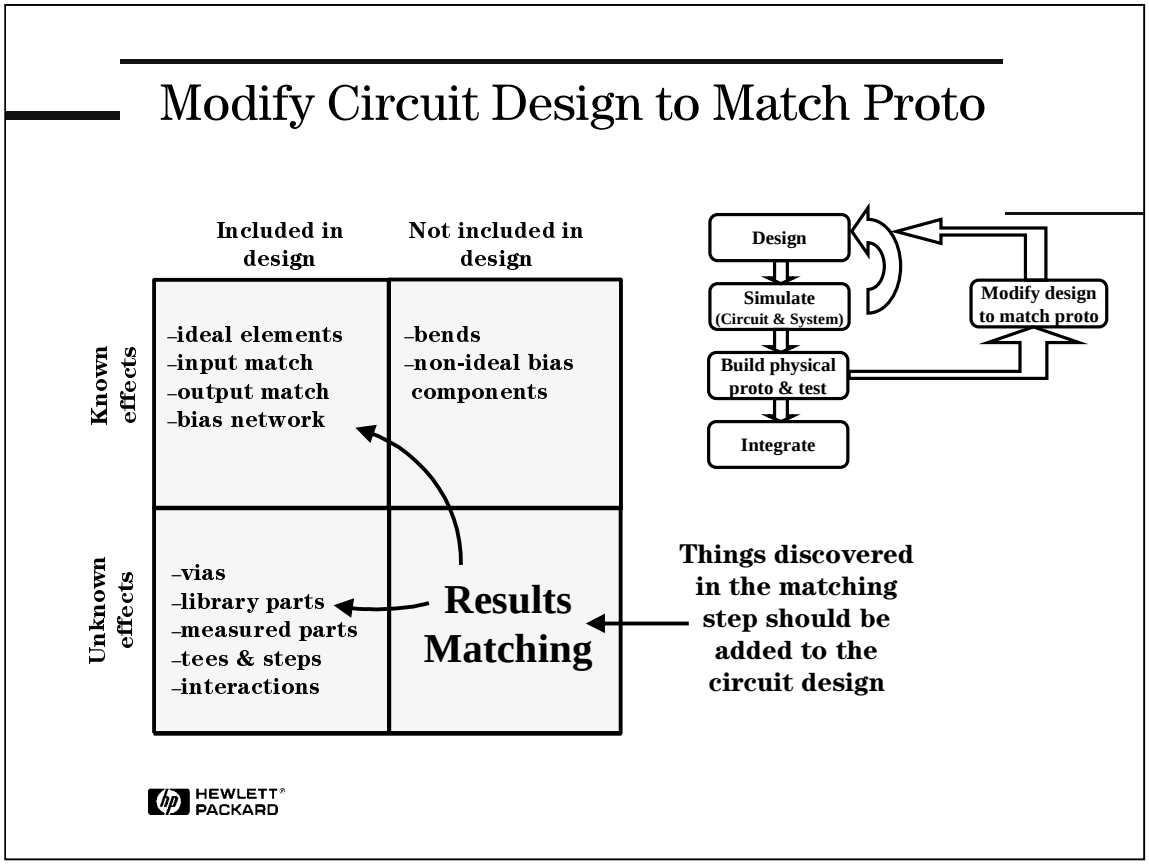
Slide #60



The physical prototype has been built and measured, but it doesn't agree with the simulated results. What happened? What you will discover is that things you either purposefully didn't include in the design had more of an effect than you expected, or that there are things that affected the circuit that you weren't aware of. The goal is to find these things, and account for them in your design with the goal of matching the simulated results to the measured ones.

It is important to keep in mind that the objective is to modify the circuit design in the software to match the performance of the physical prototype.

You can start refining the design by entering any unaccounted discontinuities or parasitics. Or in our case, check to make sure that the physical board was built as designed.

With each new discovery of an unaccounted effect, the RF designer gains experience and knowledge for future designs. If you've been able to match the simulated performance to your initial prototype, you should now have more confidence in subsequent simulations.

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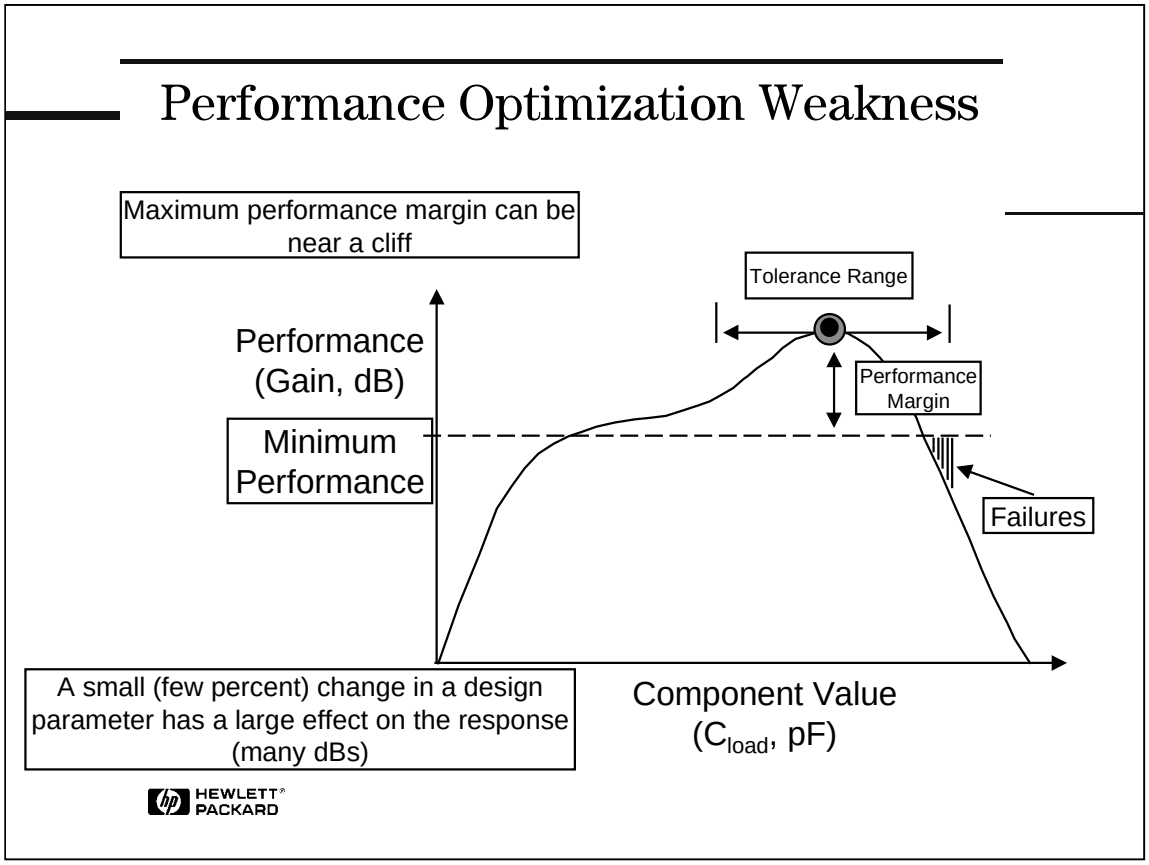
Slide #61



In the previous section, we covered the design of the LNA. We were able to build one prototype that worked. But what happens to the design's ability to meet specifications when the individual component's parameters vary within tolerance, as is the case when the design goes to high volume production?

When designs are optimized for performance, the simulated result tends toward its maximum value. In this example, as the capacitance value is increased, gain reaches a peak easily above the minimum acceptable performance level.

We may be initially very happy with the "extra" performance, but performance optimization tends to maximize the performance margin without considering manufacturing yield.

This weakness is demonstrated here when the capacitance value is allowed to vary within the tolerance range of the physical part. If the peak performance is near a "cliff," a relatively small change in value can result in a significant number of failures.

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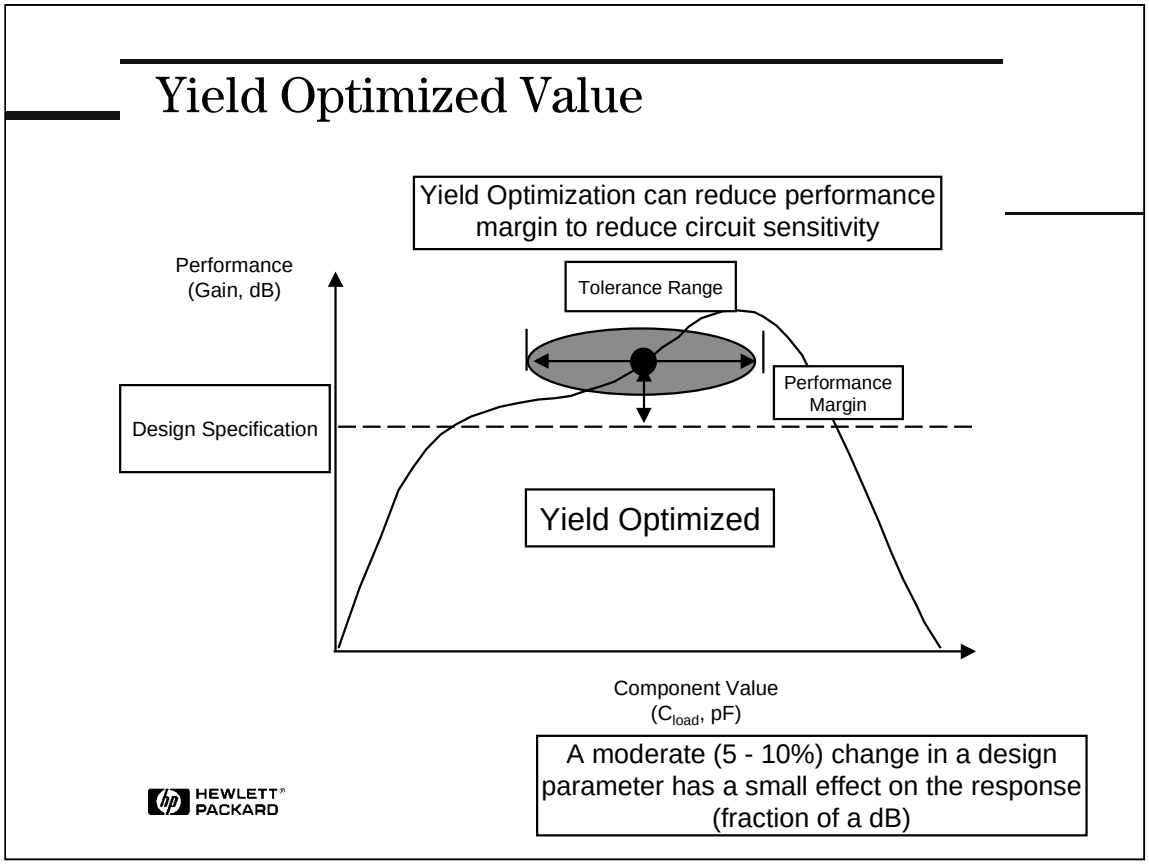
Slide #62



Yield optimization can overcome the weakness of performance optimization by taking the tolerance of the parts into consideration.

In this example, with the given tolerance range on the capacitor, yield optimization would result in a lower value for the capacitance and a lower nominal gain.

Note that the minimum performance specification is still met and the performance margin has been reduced, but we've improved the yield.

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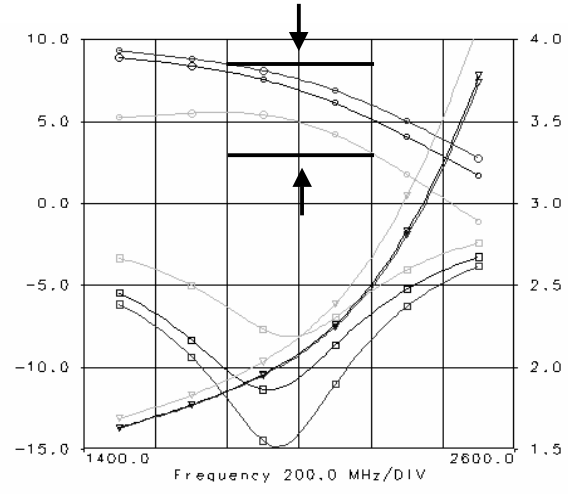
Slide #63

Yield Analysis
The Effect of Manufacturing Tolerances



When values vary within tolerance, performance can degrade significantly!

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EDA software such as HP Advanced Design System is used to analyze the yield by running hundreds or thousands of simulations allowing the parts' parameters to vary within its tolerance range according to its probability distribution function. The ratio of possible combinations of designs that pass yield goals to the total designs produced is the Yield percentage.

Here we show the S11, S22 and NF results of three simulation runs where all of the components were allowed to vary.

The random combination can lead to significant variation in performance.

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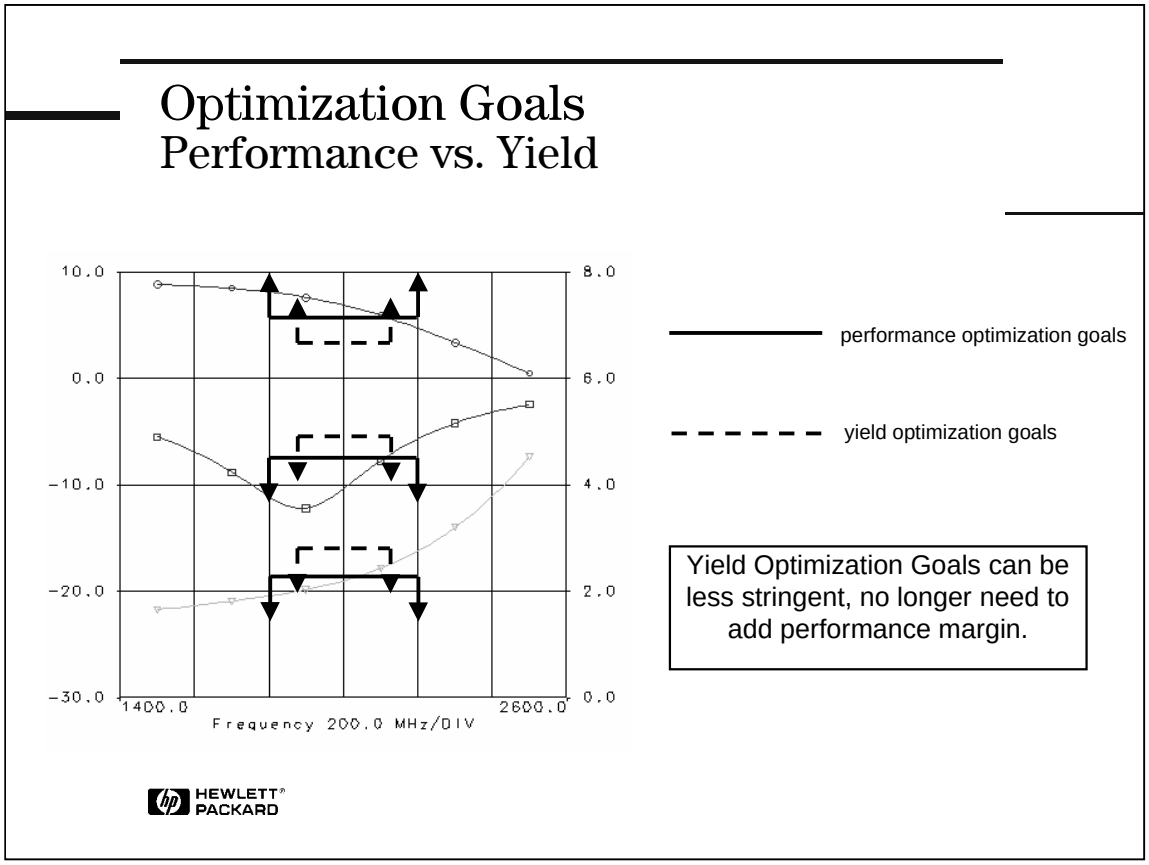
Slide #64



Like performance optimization, yield optimization needs to have a set of goals. Many designers attempt to solve the yield problem by adding a little extra performance margin when initially designing their circuits to account for part tolerances. This approach leads to specifications that are more difficult (time-consuming) to meet and may lead to more expensive parts as well. Yield Optimization goals can be set lower because if the yield is high enough, there's no need to add the additional margin.

Typical performance optimization goals are represented here by the solid lines. Performance optimization tends to force the simulated measurements to the extremes. Since a lower performance margin is acceptable if yield is improved, it is good practice to allow for this by relaxing the yield optimization goals as compared to the performance optimization goals.

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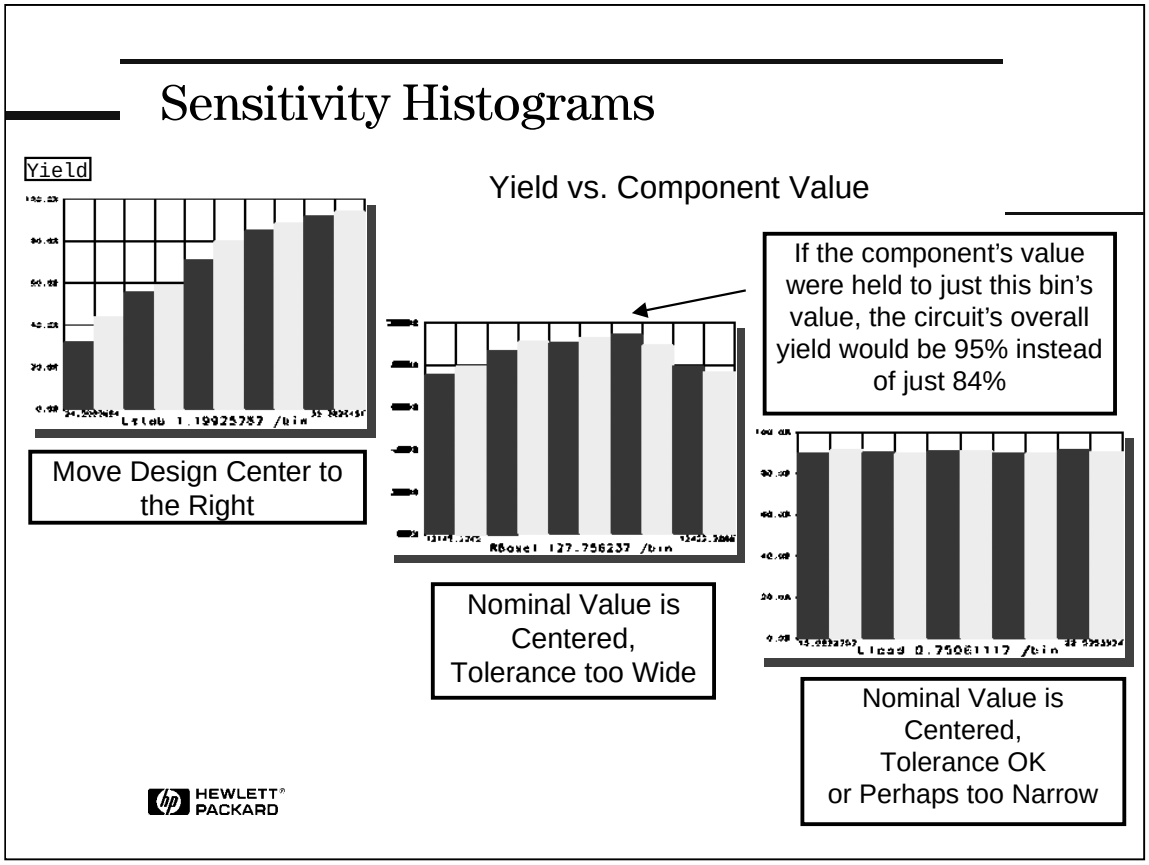
Slide #65



Using Sensitivity Histograms (SH) can increase the yield of your designs.

The value of a part is allowed to vary within its tolerance range on the x-axis. For each value of the part within, all other yield variables are allowed to vary. The yield for that "fixed" value is displayed with a vertical bar. The nominal value and the tolerance of this part can now be adjusted to improve overall circuit yield.

Yield Optimization (also called Design Centering) is the process of studying the SH and choosing the values for components that produce the greatest yield and, if needed, adjusting the tolerance of the part to increase yield.

Loosen tolerances to practical values before beginning the initial yield analysis. Then review the sensitivity histograms for potential design centering improvements.

The first SH shows that the nominal value of the part can be increased and the yield would increase.

The second SH shows that the part has a good nominal value but the yield could be improved if the part had a tighter tolerance.

The third SH shows the part that is centered, but the tolerance may be too tight. You could save on part costs by increasing its tolerance.

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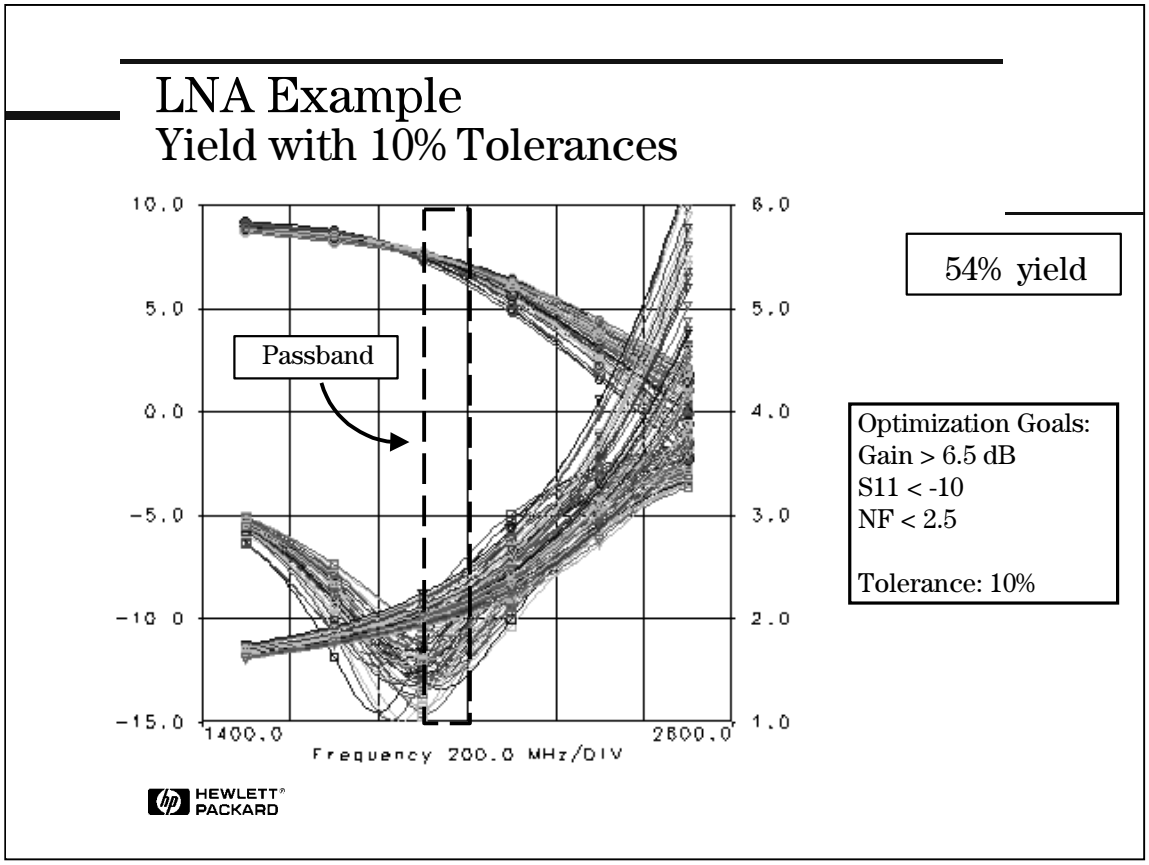
Slide #66



Here, we've taken one stage of our LNA design with part tolerances set at 5% and run a yield analysis. Even though our nominal design met specification, when those nominal values varied, our yield was 54%. This is rarely acceptable.

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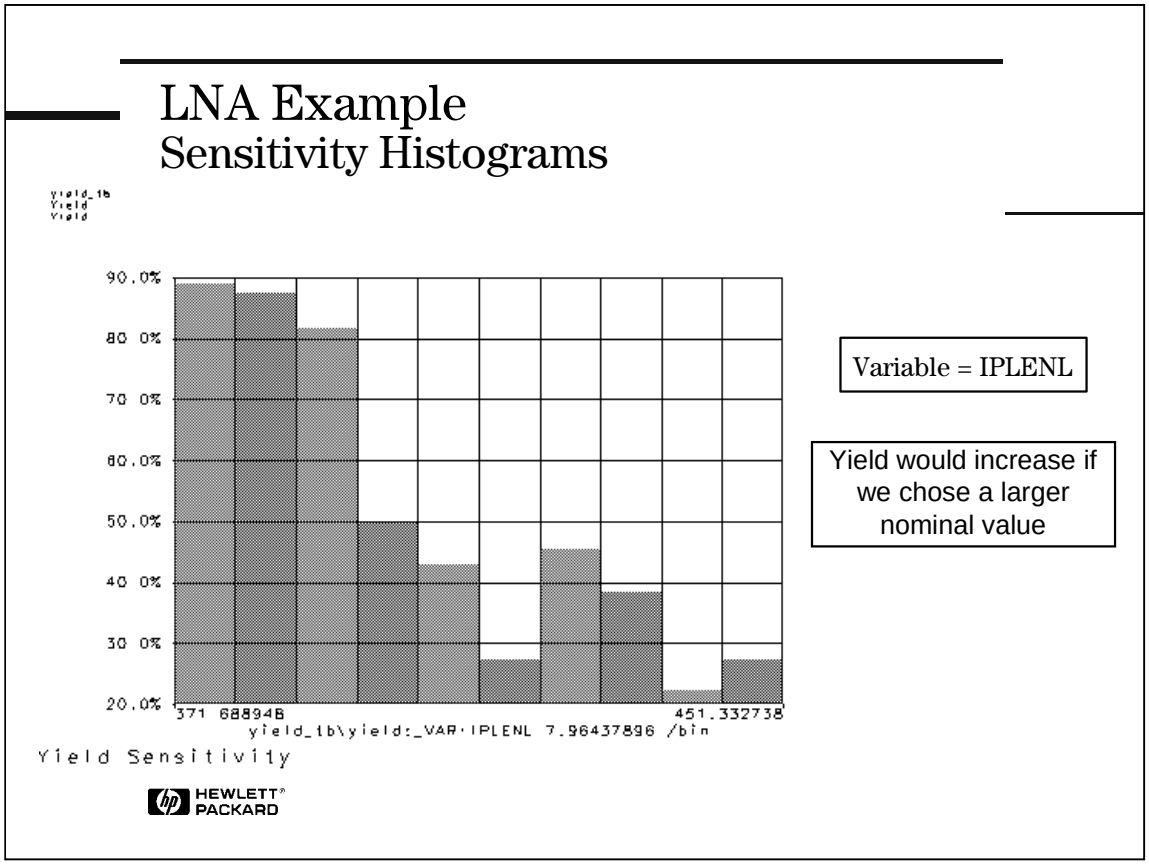
Slide #67



Examining the sensitivity histogram for the length of the matching stub shows that although the nominal value meets specification without considering tolerance, a lower nominal value would provide better yield.

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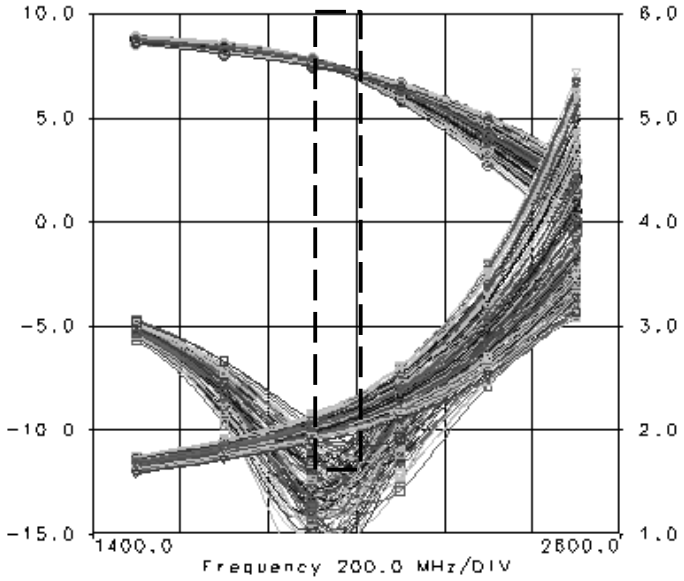
Slide #68

LNA Example
Yield After Design Centering



98% yield

After two iterations of the optimizer, the yield is dramatically increased to 98%.

Imagine now that every design block in the entire design had a similar yield. There could be dozens of design blocks. The total yield would be the individual yields multiplied together. To have a manufacturable product all design blocks must approach 100% yield.

Even if yield for each block were 99% and there were 30 such blocks, the total yield would drop to 73%.

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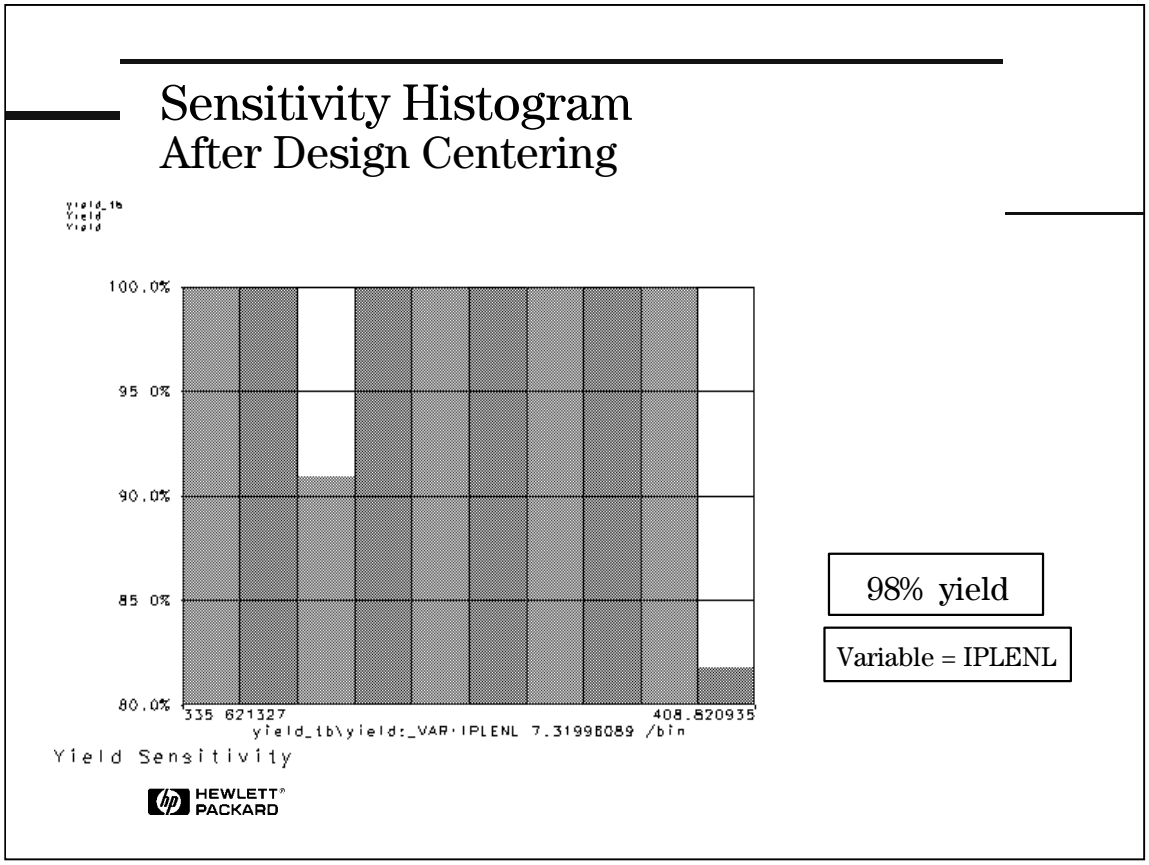
Slide #69



A re-examination of the sensitivity histogram shows that we have indeed "centered" the design. We might possibly gain an incremental improvement in yield by tightening the tolerance on the part, but considering that the yield is extremely high it is likely not worth the increased manufacturing costs to hold this item to a tighter tolerance. We have managed to raise the yield from 54% to 98% just by optimizing the nominal value and not tightening the tolerance at all.

Conclusions:

Yield Optimization by Design Centering can significantly improve overall production yield

Identify components that greatly affect yield

Make informed decisions about tolerance and nominal value

Go to production with the highest possible confidence

Resources:

Applications, Examples & Templates that make setting up common measurements easy are available at http://www.tmo.hp.com/tmo/hpeesof

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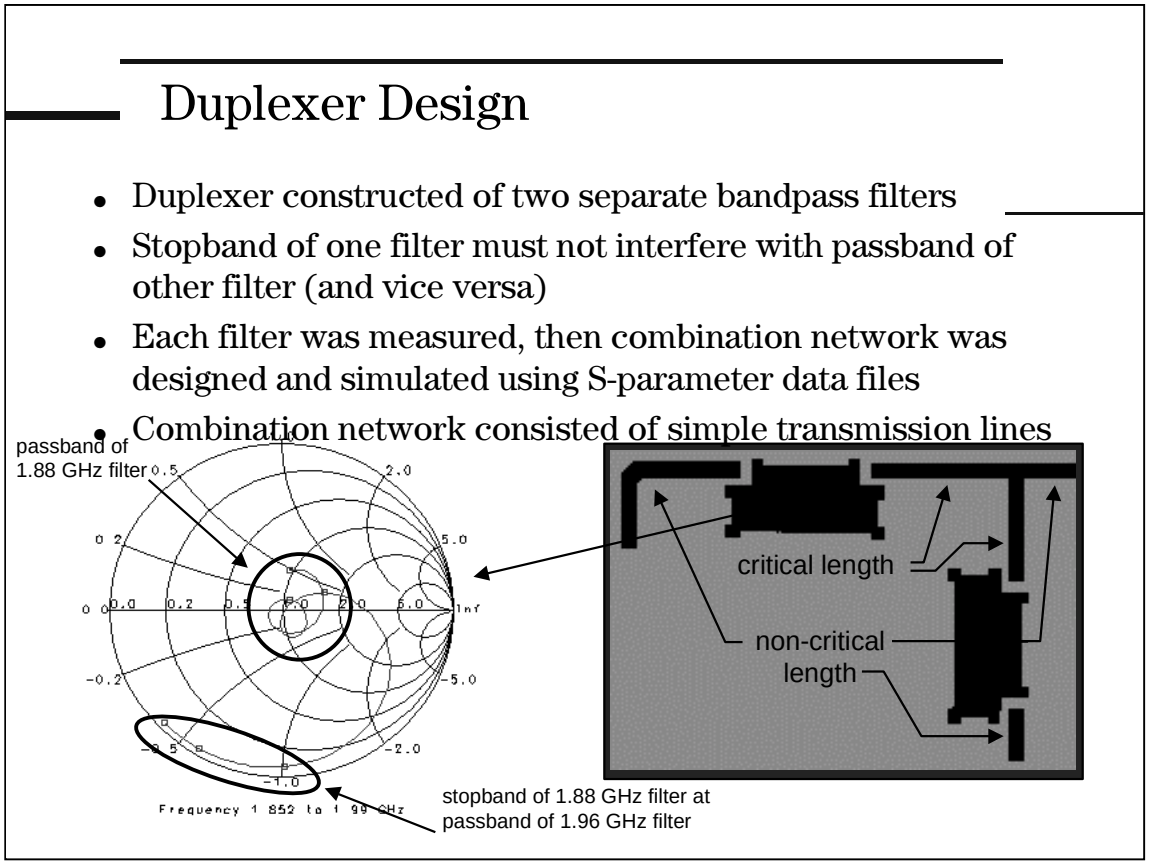
Slide #70



Now that we've completed the LNA, let's take a quick look at the duplexer. The duplexer allows the transmitter and receiver to share a common antenna. In our example, it is realized as a three-port filter that routes signals into one of two frequency bands: 1880 MHz (+/- 30 MHz) for transmitted signals, and 1960 MHz (+/- 30 MHz) for received signals. It was implemented using two separate PCS-band filters (one at 1880 MHz and one at 1960 MHz) because an off-the-shelf integrated duplexer filter could not be found.

The challenge of this duplexer design was to combine the two filters together so that the stopband of one filter did not interfere with the passband of the other filter. Since we didn't have models for the filters, the first step in designing the duplexer was to measure the individual filters with a network analyzer. We use the measured S-parameters to synthesize a combination network. The above plot of the output match of one of the filters is representative of both filters. The filters are well-matched in the passband, but highly reflective in the stopband. If the stopband of one filter looks like an open circuit at the frequencies corresponding to the passband of the other filter (and vice versa), then the filters can be combined to produce a duplexer.

Since the plot above shows that the stopband match in the critical frequency band does not look like an open circuit, we must add some line length to rotate the response to the correct impedance. This process does not affect the passband response (since it rotates around the center of the Smith chart), but it allows the stopband response to rotate to an open circuit. The necessary length of transmission line required to do this was slightly different for each filter, as seen in the above layout. After the two filters have been combined with the correct lengths of transmission line, an additional arbitrary length of 50Ω line can be added to the output without affecting the overall response of the duplexer.

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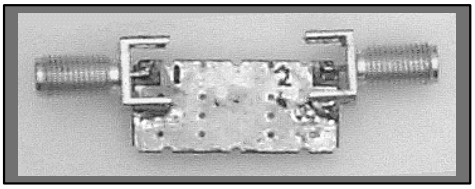
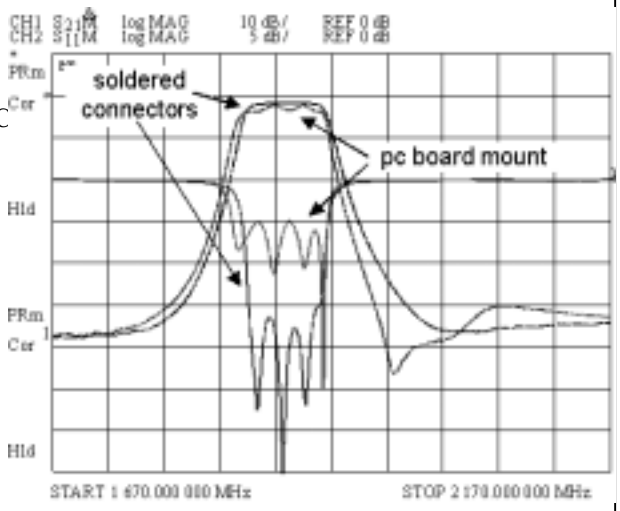
Slide #71

Duplexer Filter Measurements

- First attempt: used PC board fixture
  - Results had a lot of ripple and loss
  - Blamed on poor launches and non-50Ω transmission lines
- Second attempt: soldered connectors directly to filter
  - Response looked good
  - Will filter measure same on final PC board?





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The initial attempt at measuring the individual filters of the duplexer involved using a borrowed PCB fixture. The measured response with this fixture showed excess loss and ripple, which was attributed to poor launches and non-50Ω transmission lines. When connectors were soldered directly to the parts, the response looked much better and more closely resembled the specified response from the manufacturer. It was (incorrectly) assumed that with good launches and a proper 50Ω transmission line, the duplexer would work well on the PCB of the first prototype.

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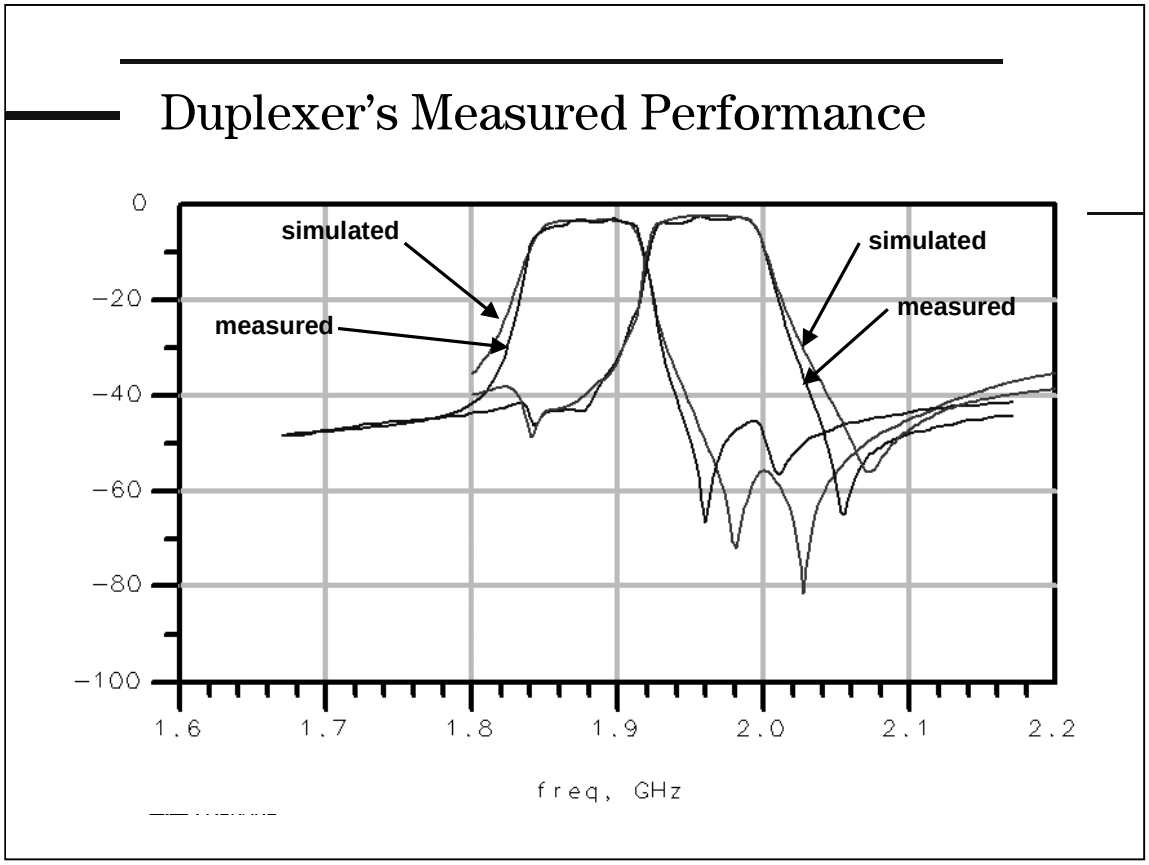
Slide #72



The above plot shows that the measured performance of the duplexer in the passband looks very much like the response of the individual filters as measured with the first PCB fixture. The simulated response shows very smooth performance in the passband. Clearly, some unknown interaction is occurring between the filter and the PCB, or possibly the filters are being damaged during the soldering process. Further investigation is needed to understand this phenomenon.